Phase C

Performance Evaluation and Optimization of the RF Circuits for a Satellite Communication System. CubeSat.

Prepared by:

Enrique Rivera

Checked by:

Approved by:

•

Institut de Microtechnique (IMT), Unine
Neuchâtel
Switzerland

•

13/09/2010

•

ESPLAB

RECORD OF REVISIONS

ISS/REV	Date	Modifications	Created/modified by
1/0			

1 FOREWORD

This report has been developed with the intention to describe the implementation and improvement design over RF system of the COM board of CubeSat. The schematics and PCB designs have been developed before within the Phase A ("Design of RF system for CUBESAT").

The already existing PCB has been mounted with components designed before and has been tested and compared the results planed against the reality, with the objective to improve them, implement the new changes and test them to acquire best results.

2 ACKNOWLEDGEMENTS:

The implementation and improvement of the RF system for CubeSat is a very interesting project; the knowledge developed has a tangible value for my future professional activity.

The project has became reachable due to the effort and support of the team of ESPLAB at IMT/Unine at Neuchâtel and Space Centre at EPFL at Lausanne, I specially thank to Prof. Dr. Pierre-André Farine and Dr. Cyril Botteron for giving me the opportunity to work with this semester project and special thanks to Frédéric Chastellain and Roman Merz for their experienced knowledge and support given to me during and out the project. I sincerely thank to Muriel Noca and Ted Choueiri from Space Center at EPFL for giving me the opportunity to collaborate with this interesting project.

Enrique Rivera

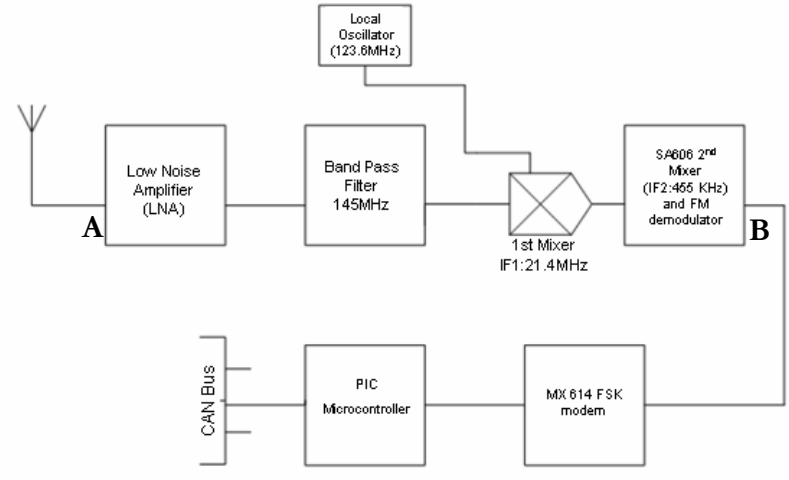
3 INTRODUCTION

This project aims to test and perform the already existing COM board of the Spacecraft system designed in the Phase A ("Design of RF system for CUBESAT").

The Objective is to implement the RF circuit on the board having the next goals:

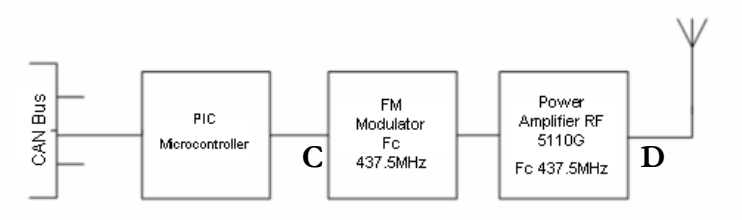
- Performance evaluation
- Identification of possible improvements of the performance or other characteristics of the RF system
- Implementation of the proposed modifications
- Complete description of all work done during this Phase

The COM Board is ready to insert on it, the components designed on Phase A. Its general architecture to be implemented is show in the next Figure



Receiver Architecture

On the reception architecture the goal is to implement and perform from the point **A** to **B**; the Microcontroller and modem are not part of the objective of this project.



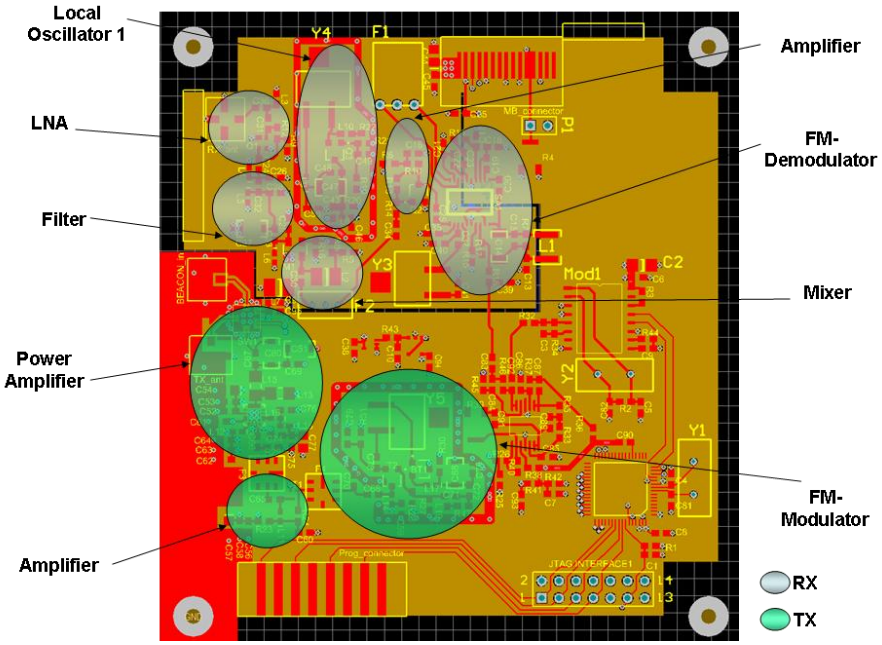
Transmitter Architecture

On the transmitter architecture the goal is to implement and perform from the point **C** to **D**; the Microcontroller is not part of the objective of this project.

Theses architectures are detailed localized in the next Figure that shows the board designed in “Altium Designer”.

The organization work on this report obeys within three important points:

- Implementation and planed results identification on “Phase A”
- Results obtained after the implementation
- Improvements, its implementation and new results



4 DESIGN REQUIREMENTS

The reference of the requirements are included in the Phase A, where it is explained the original ones that drove the design development; however in the next points are summarized the key ones that play an important roll with the objective of this project.

4.1 Power consumption

The aim is to minimize the power consumption of the RF system. The maximum power consumption of the Transmission layer is 3Watts. For the Reception layer is 70mWatts.

4.2 Frequency Operation

The Downlink frequency is fixed at 437.5MHz, and Uplink one is at 145MHz. It is important to remark that the Uplink has changed at 145.8MHz, and because of the Oscillators in existence in the Laboratory and the delay of providers, all the tests on the reception layer of the Spacecraft were made at 145MHz.

4.3 Communication Power

The Spacecraft Transmits at 27dBm and the ground station is transmitting at 43dBm. The Output power efficiency was planed on 40.8%

4.4 Noise Figure

The Signal to Noise Power Ratio at the receiver in the Spacecraft is 26dB.

5 DESIGN ASSUMPTIONS AND APPROACH

- The modulation simulated for the reception and Transmission layer was done with FSK with a data rate of 1 KHz and a frequency deviation at 1 KHz
- The injected signal as a reception input was in order of -50dBm to test the general function and parameters fixed in the original design
- In the FM-Modulator within Transmitter layer, it is assumed that the voltage to the varactor will be provided by the microcontroller. The Vpp of the data rate will be provided by the filter localized after the microcontroller's data rate output
- Maximum source of feed DC voltage is 3.3Volts

To develop successfully this project was necessary to understand the theory of each layer to identify the original requirements and to develop new designs to implement the prototype; this theory was helpful to develop the measurements in each layer to evaluate the results and to identify the improvements implemented and evaluated, in this project.

6 TECHNICAL DESCRIPTION AND TESTS

The technical description and tests results have been included in one section with the objective to explain in this order the expected and real results and afterwards the improvements implementation.

6.1 Receiver

The project starts with this layer taking in consideration the priority and the complex work behind of the design of a Low Noise Amplifier.

6.1.1 LNA

The first approach was to test the LNA with an uplink frequency of 145 MHz. The first circuit's implemented and tested is shown in figure 1. (To see the larger images it is recommended to go to the PCB file, Version 4 included in the CD of this project where all circuits are available. Or at the end of this report are larger images of each architecture)

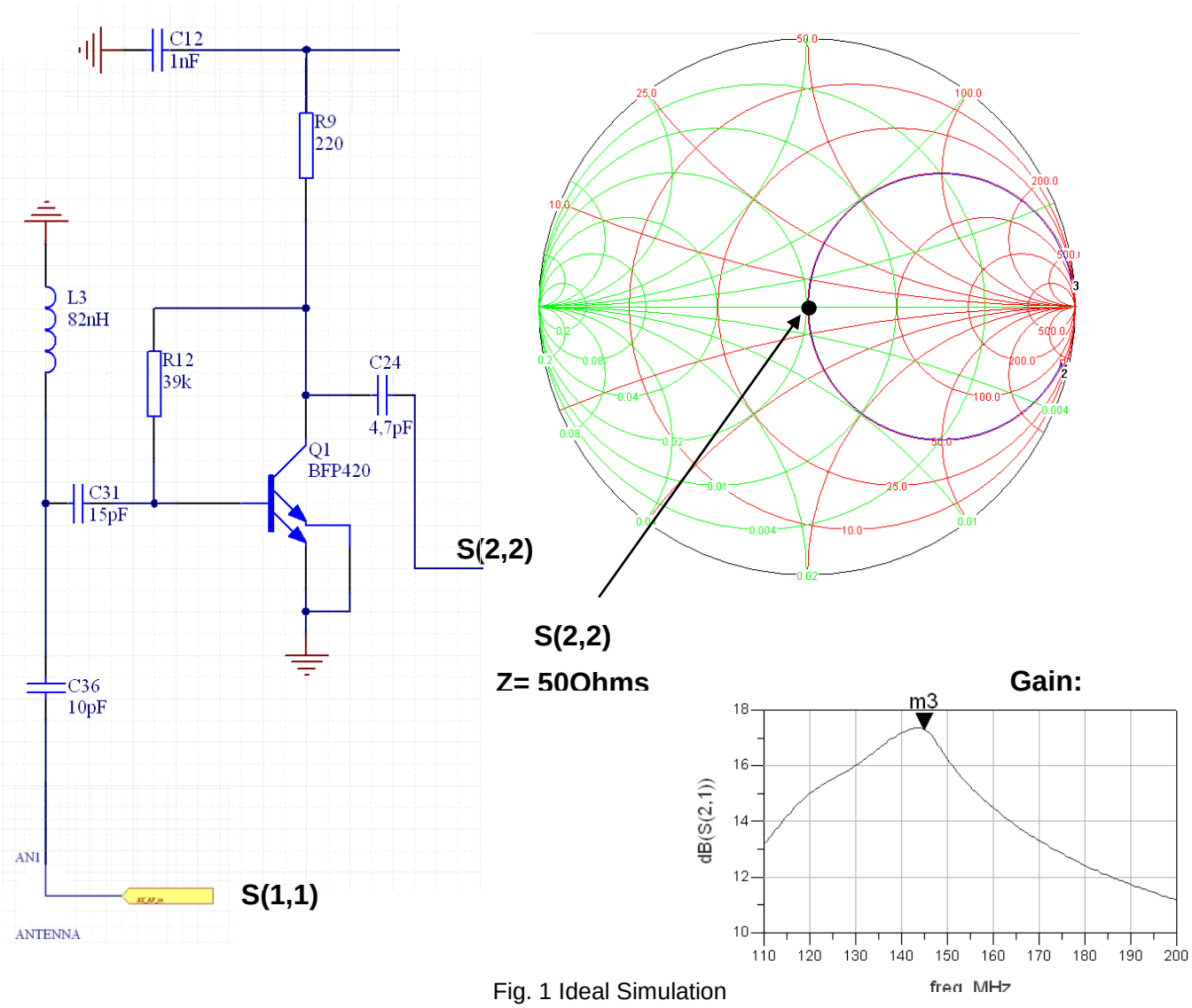


Fig. 1 Ideal Simulation

As it is shown in last Figure, **the goal was to match the impedance at the output at 50 Ohms, getting the maximum gain compared between S(2,2) and S(1,1).**

6.1.1.1 DC Analysis

The first analysis done was the Direct Current evaluation. The current designed at the collector was less than 3 mA with a Vdd of 3.3V. In the real scenario with a R9 of 220 Ohms and a Vout of 2.636 Volts, the collector current (Ic) was 3.018mA. R12 had a first value of 39Kohms. The hFE obtained was 92, the specified in data sheet was typically in 100. To reduce the current, it was necessary to made constant the value on R9, and calculated the value of R12. Applying the Kirchkof's voltage law: Vout – Ibase*R12 – 0.7=0. The DC Vout designed was 2.636 Volts. It is known that Ibase= Ic/hFE and due to this last formula R12 calculation was 60 KOhms. The real value was 68 KOhms because of the commercial values in the laboratory. Then the real results with these changes were***: R12= 68KOhms, Ic=2.86mA and Vout= 2.66Volts.***

6.1.1.2 AC Analysis

The second analysis was the small signal one. AC analysis consisted in two parts. The first one was the input test finding out impedance matching at 50 Ohms. The second one, was to test the complete network and maximize the gain between the input and output due to the impedance matching of the network.

6.1.1.2.1 Input

At the first part (Input), the capacitor C31 was fixed with a value of 22pF. The equivalent circuit simulated is showed in figure 2.

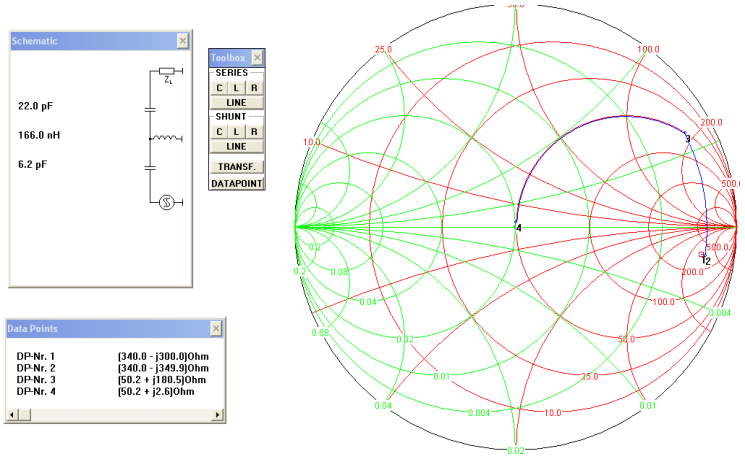


Fig. 2 Simulation

Within the simulation done in the last figure, instead of C36 it was implemented a resistor of 0 Ohms. The impedance at S11 with L3 in open circuit was 340-j300. After that, this impedance was calculated to be approached at 50 Ohms in the Smith cart curve due to the value of L3. This inductance obtained was L3= 150 nH. The impedance point was 50+j149. Then last calculation implemented was C36 to drive the complex impedance to cero, the value of C36 was 5.6pF. The real scenario is shown in Figure 3. As it is shown in Fig. 3, the matching was not perfect; as the LNA is a feedback system, before to continue to work only with the input, the next step was to include the output.

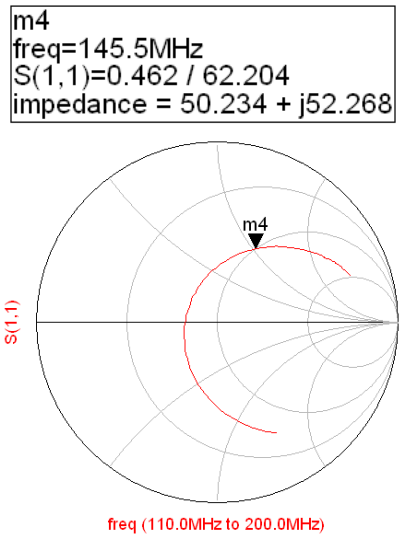


Fig. 3 Real Results

6.1.1.2.2 Output

In the second part (Output), the simulation has been modeled with C24 and an inductance in series because of at the first testing there was a large attenuation. First of all a resistor of 0 Ohms was used instead of the capacitor C24. A new capacitor between collector and ground was inserted, the value

calculated was 1.8pF. The impedance point was 53-j57. Going forward, the inductance in series has been calculated at 91 nH. The capacitor in series after the inductance was modeled with an elevated value to no change the last coupled impedance. The system modeled is shown in figure 4.

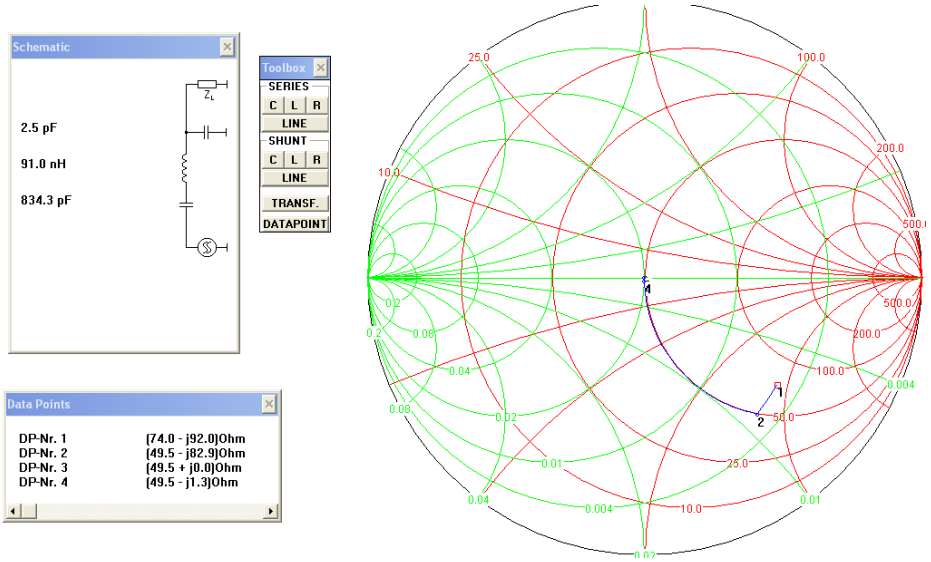


Fig. 4 Simulation

The real scenario is shown in figure 5.

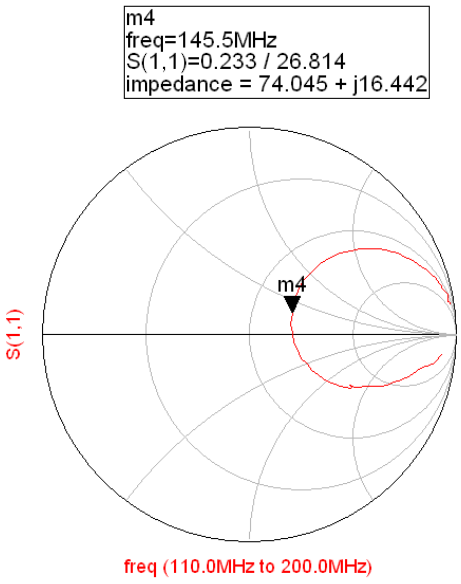


Fig. 5 Real Results

6.1.1.2.3 All Network

As we can see in the last Figure the marker m4 localized at 145MHz has a mismatch with the 50Ohms curve of the cart. After this second part, as it is mentioned before, the input has been modified by the output; it means that is a feedback system. Taking in consideration the deviation provided by of the output modifications and trying to have the best matching and maximal gain the results were: ***L3= 270 nH, C36= 2pF and C31=22pF***. The real scenario is shown in figure 6.

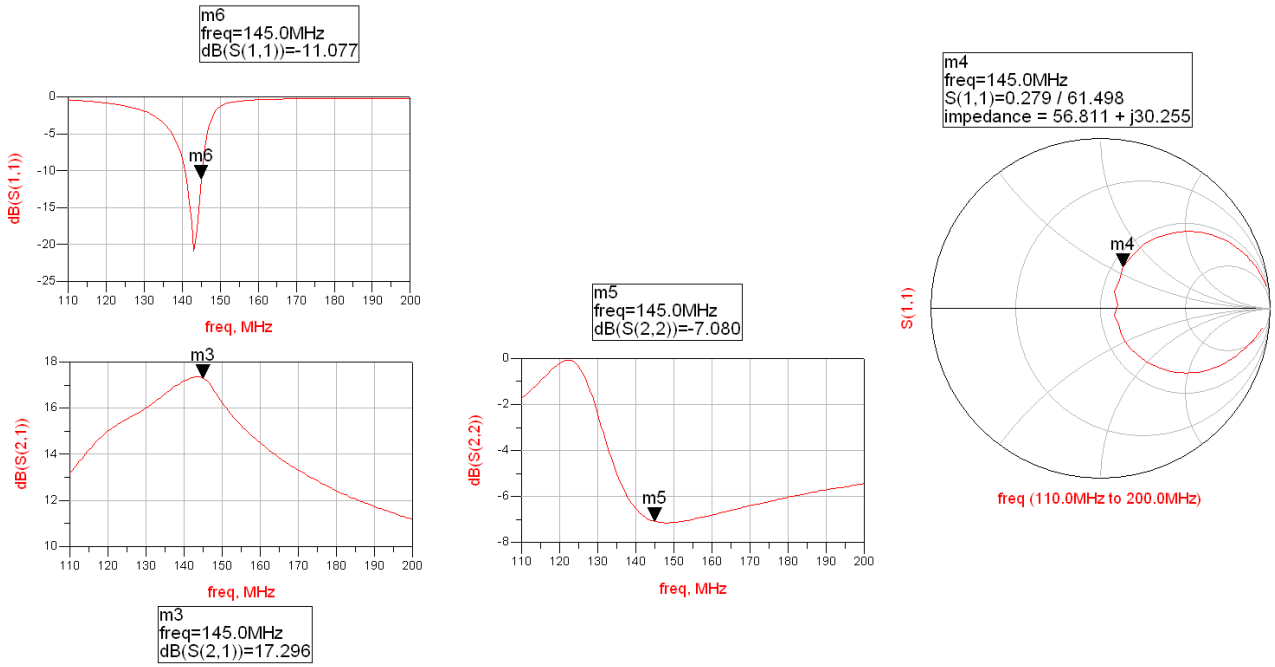


Fig. 6 Real Results

As we see in Figure 6, the maximum gain was in 17.3dB, having a deviation of -4.7dB from the original circuit. The reason of this deviation is in function of the ideal scenario on the simulations and the real parameters of transistor and passive components.

The Final Circuit updated in Altium Designer is shown in the Figure 7; the PCB has been modified too.

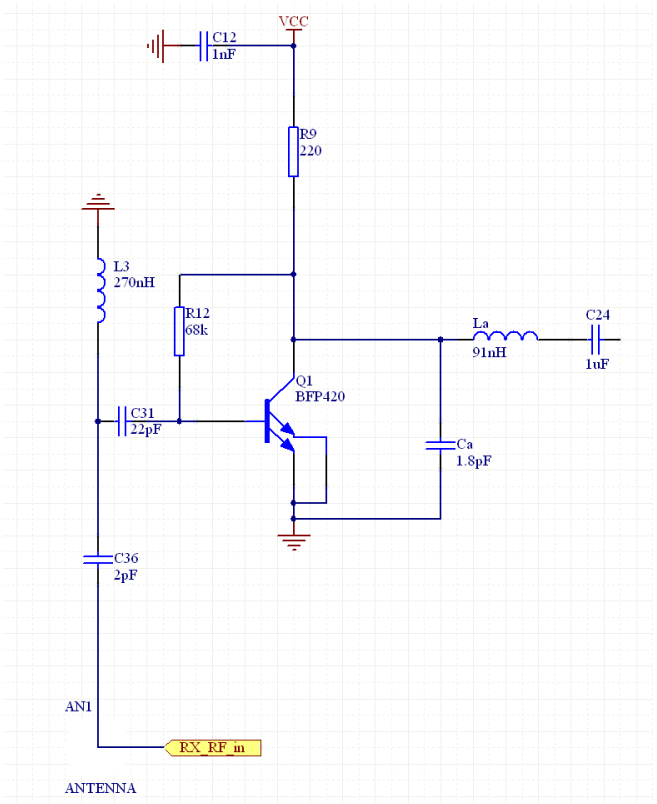


Fig. 7

6.1.1.2.4 Noise Figure

One of the most important parameters to be measured in a LNA circuit is the Noise figure. It is known that the Noise Figure is the ratio between SNRin and SNRout in a logarithm scale, it means in dB. It is important to mention that the original design has not included the SNR analysis then there were not parameters to compare.

To measure the noise in the laboratory was a challenge; for this reason a Faraday Cage was used to ensure the real noise produced by the LNA.

At the input, an average of noise was measured at 77nVolts with an input signal generated at 186nVolts and 145MHz; the square relationship between these figures gives the SNRin that was 5.84. The spectrum representation is shown in Figure 8.

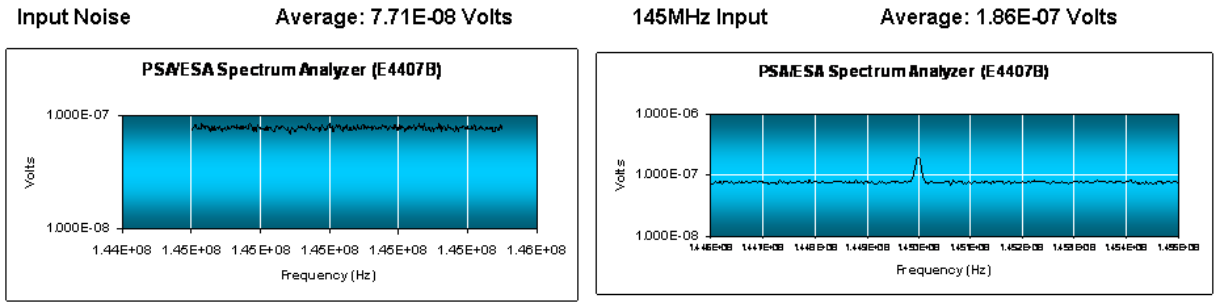


Fig. 8

In the output case, an average of noise of 746nVolts was presented, with an output signal amplified of 1.47uVolts at 145MHz; the square relationship gives the SNROut that was 3.86. The SNRin is better that the SNROut, it is normal due to the amplification and the addition noise by the LNA. The spectrum results are shown in Figure 9.

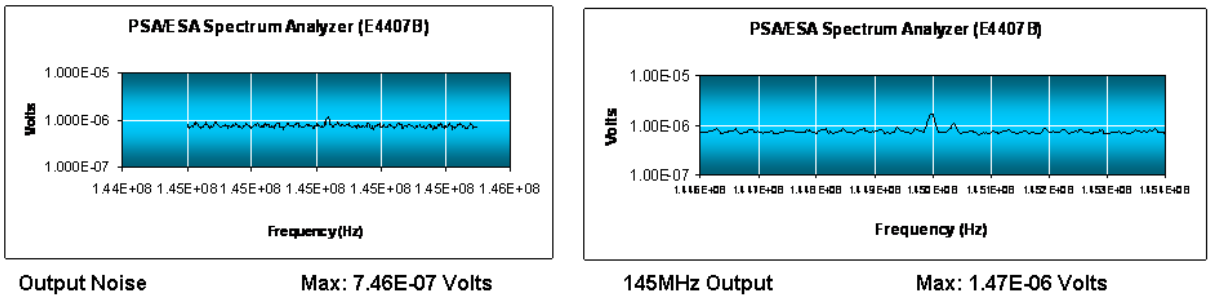


Fig. 9

The Figure Noise is calculated in a dB scale due to the ratio between SNRin and SNROut. This result was around of 2dB. It means that the LNA is producing a noise of 2dB, and it is in range of the industry market that presents figure noise from 2 to 5 dB.

In the Figure 10, are shown the noise figure calculations.

	Average		RMS	
	Amplitude	Units	Amplitude	Units
Input Signal	1.86E-07	Volts	1.86E-07	Volts
Input Noise	7.71E-08	Volts	7.71E-08	V_{RMS}
SNR Input	**5.84**		**5.83**	
Output Signal	1.47E-06	Volts	1.47E-06	Volts
Output Noise	7.46E-07	Volts	7.49E-07	V_{RMS}
SNR Output	**3.86**		**3.83**	
Signal Gain	7.870		7.870	→ **17.920 dB**
Noise Gain	9.683		9.715	→ **19.720 dB**
SNRin/SNRout	**1.80**	**dB**	**1.83**	**dB** → **1.800 dB**

Fig. 10

LNA is concluded with a maximum gain of 17.26dB and a Noise Figure of 2dB. The Power consumption was tested at 90mWatts.

6.1.2 Band Pass Filter

In this section **the goal was to have a filter with the lowest loss insertion at 145MHz.** The simulation has provided an attenuation of 1.37 dB, the minimum insertion reached, changing the capacitance of 24pF into a 4.3pF. The real scenario with these capacitances is presented in Figure 11.

The Input at point a) in the Figure 11 correspond to the output of the LNA that was the resultant of inject a -50dBm signal at the LNA input, and considering the gain of17.26dB the power at point a) was -33dBm. **The real insertion was neglected since the output at point b) was -31.2dBm.**

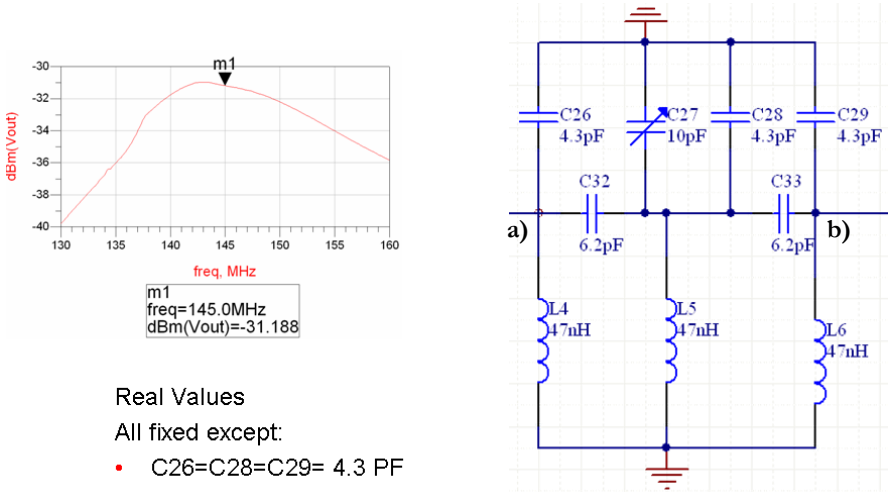


Fig. 11

6.1.3 First Mixer and Oscillator

In this part, **the goal was to ensure the oscillation frequency in the Oscillator circuit at 123.6MHz, to have as a result of the multiplication with the carrier at 145MHz, the first IF at 21.4MHz.** Figure 12 shows the simulation of the mixer circuit at these frequencies mentioned.

imt

Mixer Simulation

Enrique Rivera December 07

Amplitude			
-38	dBm	1.58E-07	Watts
12	dBm	1.58E-02	Watts

Frequency In	145	MHz		
Osc Frequency	123.6	MHz	Phase change	0 °

Frequency Out	**21.4**	**MHz**

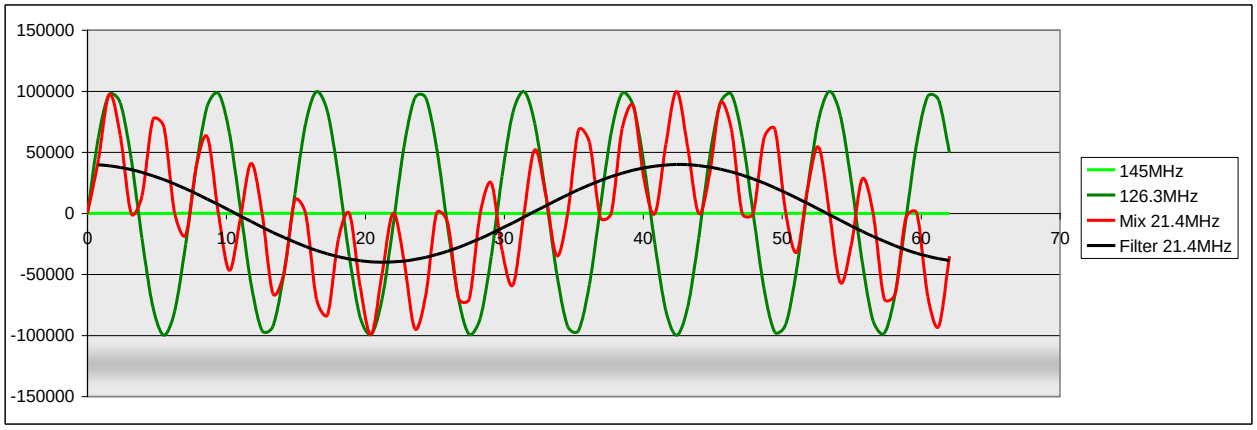


Fig. 12

This circuit has functioned at the first implementation, having only one change in the coupling capacitance C43. The results are shown in Figure 13.

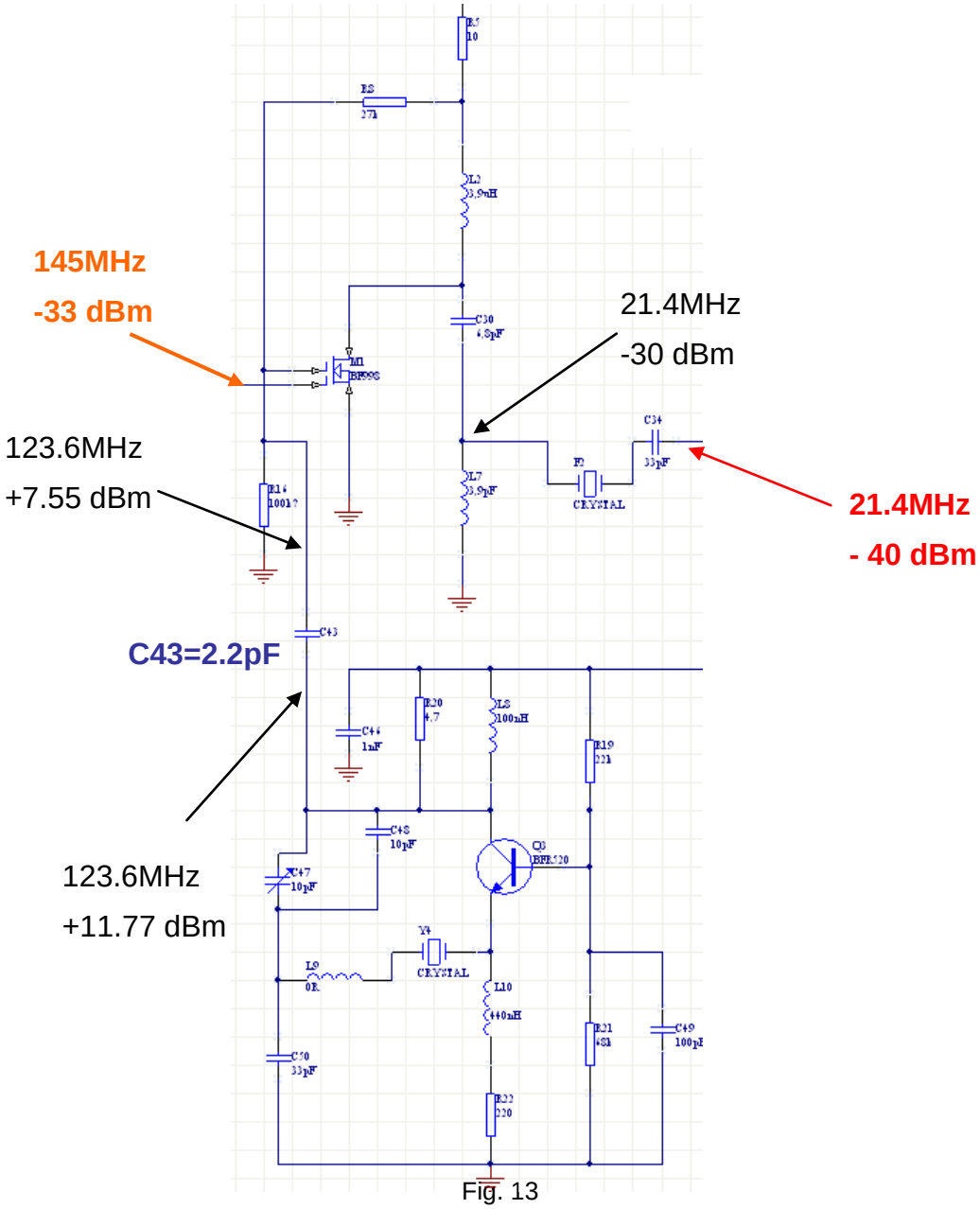


Fig. 13

The output signal was exactly at 21.4MHz with a power of -40dBm. The injection signal at the input of the LNA was in order of -50dBm having at the input of the mixer -33dBm. The spectral result is shown in Figure 14.

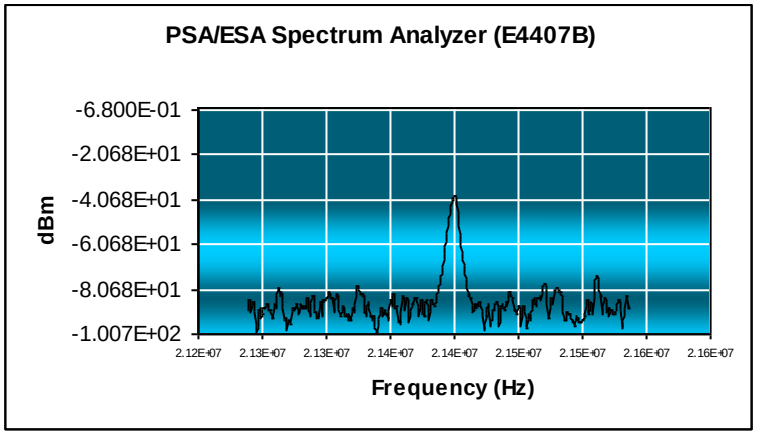


Fig. 14

The planed result was in -49dBm of output power having a difference with this implementation of +9dB. It is important to remark that if the Uplink frequency changes from 145MHz to 145.8MHz, it is necessary to provide the oscillation frequency at 124.4MHz of the crystal, to ensure the same IF at 21.4MHz.

6.1.4 Amplifier

As it is shown in last section, the output signal of the First Mixer was in order of -40dBm of power then it is necessary to amplify this signal. An amplifier has been implemented the amplifier shown at Figure 15.

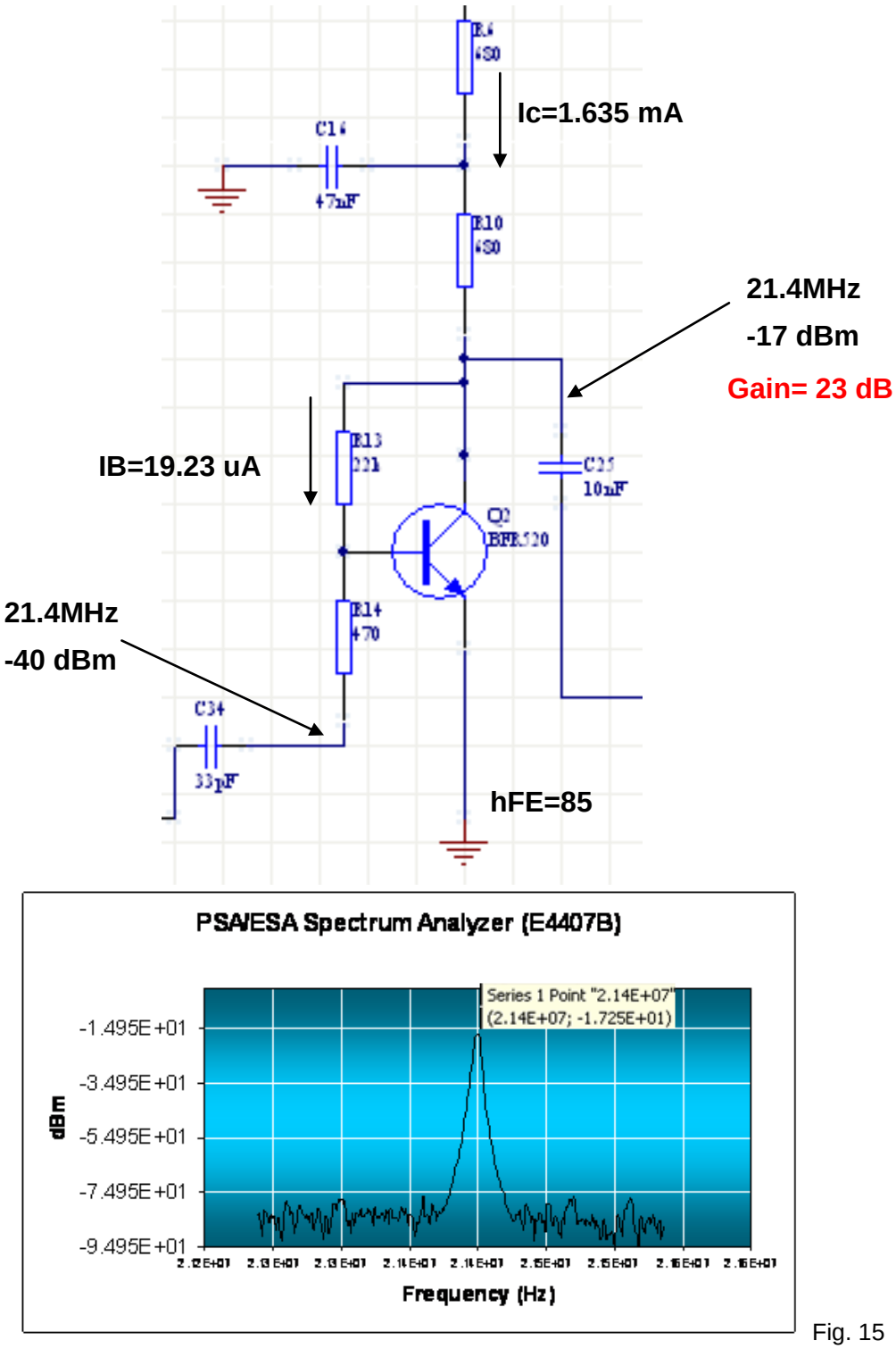


Fig. 15

The goal at the simulation was to have a gain of 17dB. At the real scenario it is found a gain of 23dB, making a result of -17dBm at the output. This circuit was not simulated in Phase A.

6.1.5 FM-Demodulator

This circuit has **the goal to demodulate the signal over the IF of 21.4MHz**. To do this was necessary to make a second down conversion from 21.4MHz to 455 KHz.

As shown in Figure 16, the first part of the IC SA606 makes the second down conversion. The result at pin 18 was a sinus signal of -11dBm and with a frequency of 455 KHz that needs to be amplified and the pass to the limiter to convert it into a square signal.

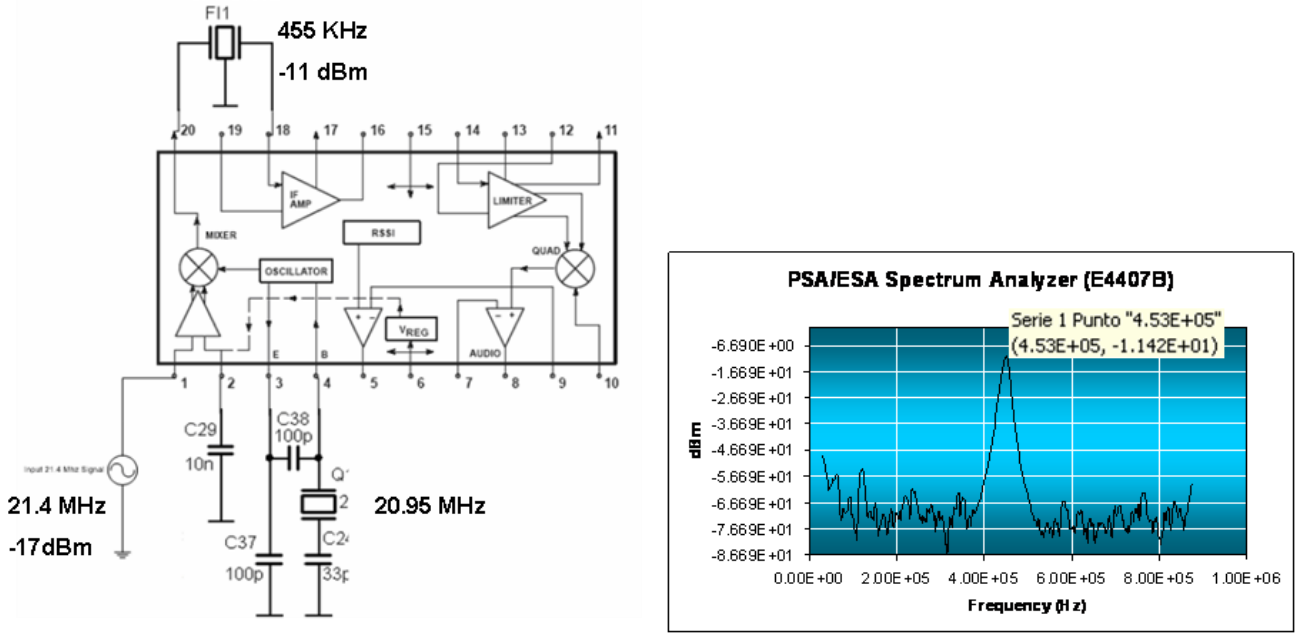


Fig.16

This circuit uses a Quadrature demodulation that needs at the input of the QUAD the square signal and the same signal but shifted 90° to make the demodulation. To do this shift phase, was necessary to calculate the resistance R7 shown in Figure 17. **In Phase A this resistor was designed as no connection point, but as mentioned before, it is necessary to generate the 90° of phase shift.**

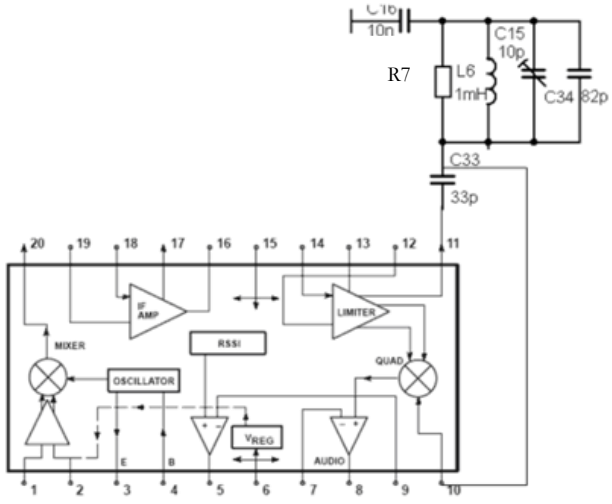


Fig.17

The calculation of R7 was simple. First of all, the total capacitance equivalent in the circuit has been calculated: Addition of 5PF (variable capacitance), 82pF and 33pF. The total capacitance was 120pF. To manage the working frequency at the QUAD, it is necessary to understand the equivalent circuit described in Figure 18.

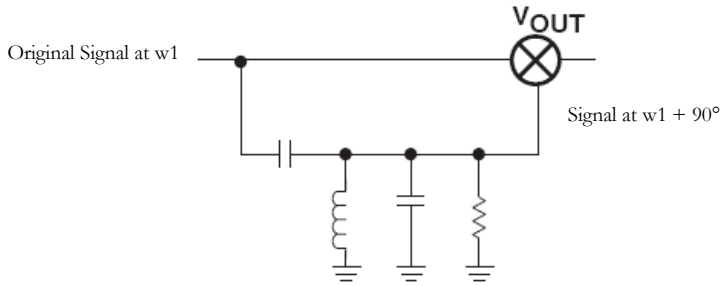
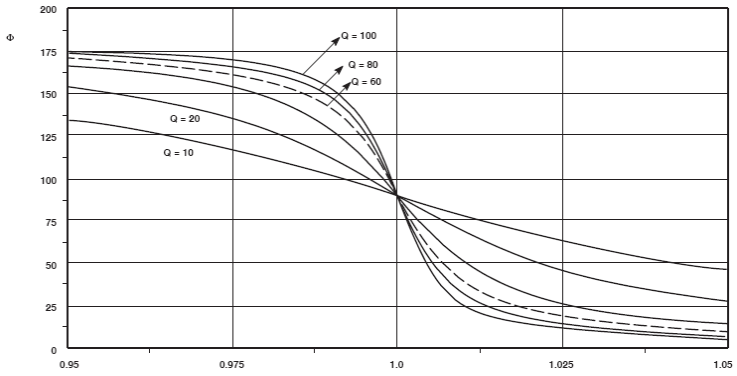


Fig. 18

The calculation of the frequency is in function of the total capacitance and the inductance:

$$\omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad \text{... Eq. 1}$$

Knowing the value of frequency (f) at 455 KHz, then w1 is defined by 2PI*f that was 2.86KRad/seg. Using the Equation 1, it is shown that the inductance was right calculated before at 1mH. To calculate the resistance was necessary to consider of one of the most important characteristics of the QUAD modulation, the loaded Q of the quadrature tank, that impacts in three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are shown in Figure 19. The phase angle translates to a shift in the multiplier output voltage.



Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

Fig. 19

The better Q to work is the one more linear as Q=10 or 20 that gives to the output more stability, but working with lower Q decreases the amplitude of the output signal, then a Q of 20 has selected to calculate R due to the formula:

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad \text{... Eq. 2}$$

Using the Equation 2, the resistance was calculated at 58 KOhms. Because of the commercials resistors in the laboratory a value of 56 KOhms was used.

To test the circuit, it has been injected a square signal FSK modulated with rate at 1 KHz and a deviation function of 1 KHz within the carrier at 145MHz at the input of the LNA. The output at SA606 was a square signal with rate at 1 KHZ and 155mVpp, shown in Figure 20. It demonstrates that the circuit works successfully.

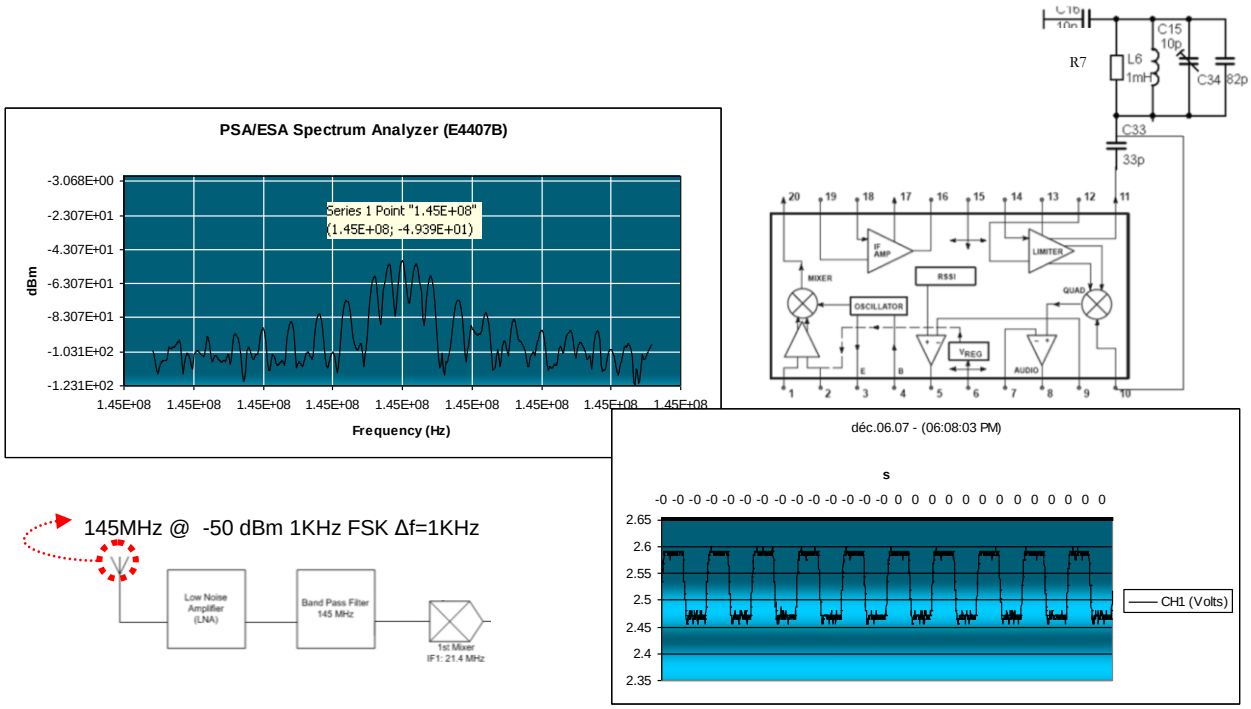


Fig. 20 1KHz 155 mVpp

The output signal has not been modelled in the original design then there was not parameter of comparison.

6.2 Transmitter

Taking in consideration that the Power Amplifier is the most key circuit to reach a maximum Downlink transmission power, the implementation started with this circuit.

6.2.1 Power Amplifier

The most important points to manage of this circuit are:

- **Voltage Amplifier Power Control (VAPC)**
- **Minimum input power to activate the maximum transmission power**
- **Maximum Output Power in function of output current**

In Figure 21 illustrates these target points in the circuit.

These points are detailed in the Appendix A where it is the data sheet of the circuit RF5110G. The central points of this implementation were the Inductances L13 and L15 with low DC resistance to support the maximum current at 1 Ampere and generate lowest loss insertion. The original design did not contemplate the Ferrite L18, and it is important to be considered because of the Pin 5 and 6 are the feed DC voltage of the two first amplifiers stages in the IC RF5110G, as well as provide some frequency selectivity to tune to the operating band. The value of this Ferrite was taken from the application schematic from its data sheet that was at 10Ohms with a Murata's code of LQH32CN331K23L. The space over the PCB was not sufficient to place this Ferrite (L18) then was necessary to modify the PCB for the future work. In the other hand, the L13 placed on, has been chosen having the lowest DC impedance value to compensate the loss insertion produced by the maximum current at 1 Ampere; this inductance was LQW31HN39NJ03L from Murata with a DC resistance of 0.067 Ohms. The same analysis has been done for L15, but in this case the *ceramic* inductance had better response in order to achieve the maximum output power.

Overview:

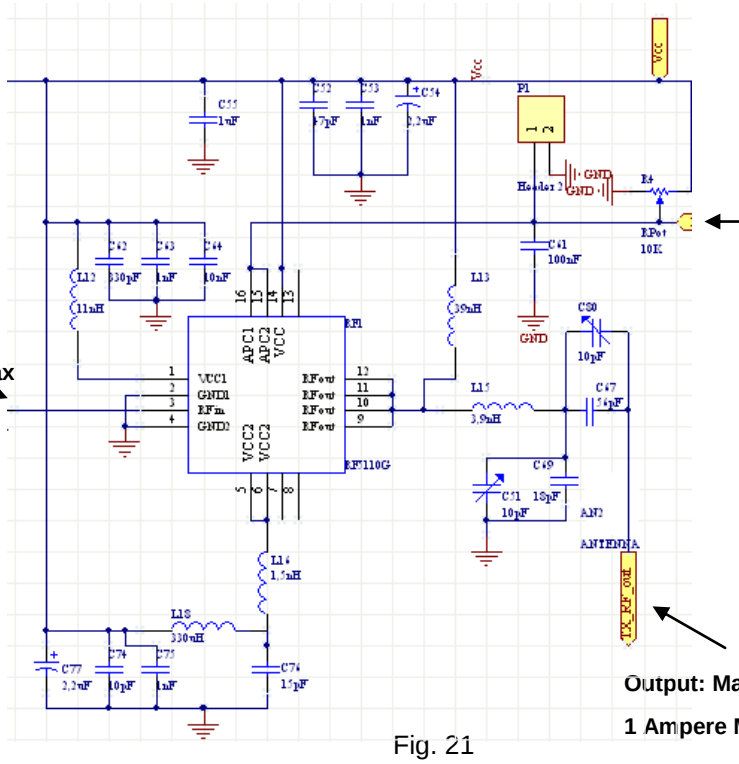


Fig. 21

Regarding the data sheet, the maximal output power is reached when the Voltage Amplifier Power Control is at 2.8 Volts and the input signal power is at 4.5dBm.

To test this Maximum Output Power was necessary to fix VAPC at 2.8 Volts and to vary the input power (Pin) as shown at Figure 22.

VAPC=2.8 Volts					
Input		Gain		Output	
-15	dBm	36	dB	21.4	dBm
-14	dBm	36	dB	22.3	dBm
-13	dBm	36	dB	23.3	dBm
-12	dBm	36	dB	24.3	dBm
-11	dBm	36	dB	25.1	dBm
-10	dBm	36	dB	25.9	dBm
-9	dBm	36	dB	26.7	dBm
-8	dBm	36	dB	27.6	dBm
-7	dBm	35	dB	28.3	dBm
-6	dBm	35	dB	29.1	dBm
-5	dBm	35	dB	29.8	dBm
-4	dBm	34	dB	30.3	dBm
-3	dBm	33	dB	30.4	dBm
-2	dBm	33	dB	30.6	dBm
-1	dBm	32	dB	30.6	dBm
0	dBm	31	dB	30.7	dBm
1	dBm	30	dB	30.7	dBm
2	dBm	29	dB	30.8	dBm
3	dBm	28	dB	30.9	dBm
4	dBm	27	dB	31.0	dBm
5	dBm	26	dB	31.2	dBm

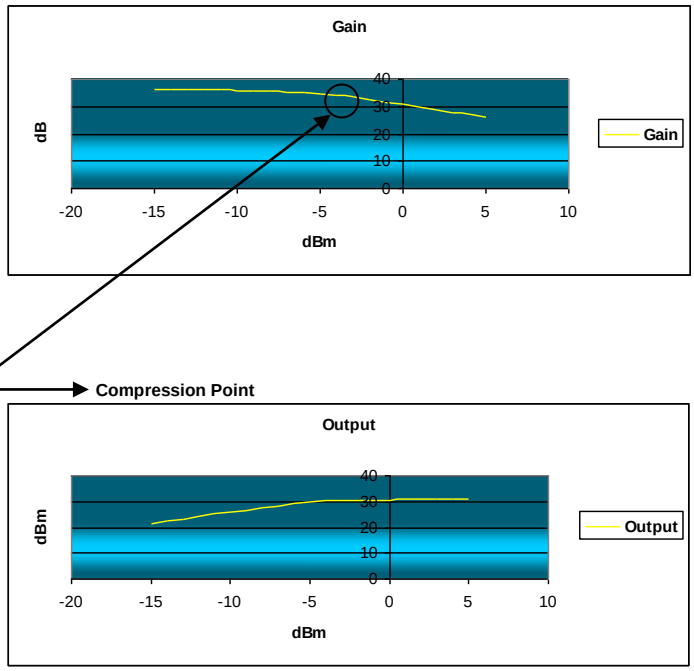


Fig. 22

As expected, the maximum power is reached between 4 and 5dBm at the Input and the compression point is reached at -5dBm, where the gain starts to decrease and the output power becomes constant. **It is important to mention that the maximum power was not 32dBm, the result was 31dBm, having a difference from the data sheet of -1dB.**

The Output efficiency has been calculated making the ratio between the Power at the output and the power consumption of the Power Amplifier**.** The result of the efficiency analysis is shown in Figure 23.

VAPC=2.8 Volts			
Input (dBm)	Pout (Watts)	Pconsumption (Watts)	Efficiency
-15	0.1	1.0	13%
-14	0.2	1.1	15%
-13	0.2	1.3	17%
-12	0.3	1.4	19%
-11	0.3	1.6	20%
-10	0.4	1.8	22%
-9	0.5	2.0	24%
-8	0.6	2.2	26%
-7	0.7	2.4	28%
-6	0.8	2.4	34%
-5	1.0	2.5	38%
-4	1.1	2.7	39%
-3	1.1	2.7	40%
-2	1.1	2.8	41%
-1	1.1	2.8	41%
0	1.2	2.8	41%
1	1.2	2.9	41%
2	1.2	2.9	42%
3	1.2	2.9	43%
4	**1.3**	**2.9**	**43%**
5	**1.3**	**2.9**	**45%**

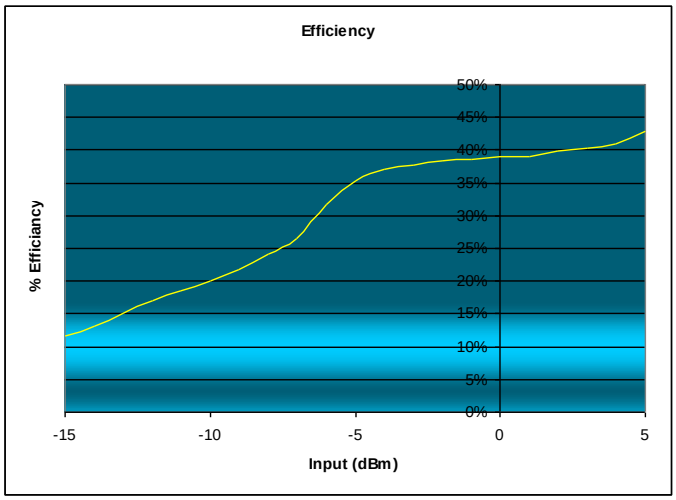


Fig. 23

The maximum efficiency mentioned in the datasheet is about 57%. It is clear that the maximum achieved was near to 43%, having a difference of -14 percentage points.

Other point of view of the power consumption analysis was consisted in fixing the Input power at 4dBm and varies VAPC. **The maximum power was reached at 0.88 Amperes instead of 1 Ampere then the maximum power dissipation in function of Vcc at 3.3 Volts was 2.9 Watts.** In Figure 24 the results are shown.

Input 4dBm	
VAPC (Volts)	**Current (A)**
0.00	0.001
0.10	0.001
0.20	0.001
0.30	0.001
0.40	0.001
0.50	0.001
1.00	0.011
1.10	0.021
1.20	0.034
1.30	0.045
1.40	0.065
1.50	0.092
1.60	0.095
1.70	0.095
1.80	0.093
1.90	0.099
2.00	0.108
2.10	0.115
2.20	0.121
2.30	0.132
2.40	0.175
2.50	0.770
2.60	0.830
2.70	0.870
2.80	**0.880**
2.90	0.900
3.00	0.910

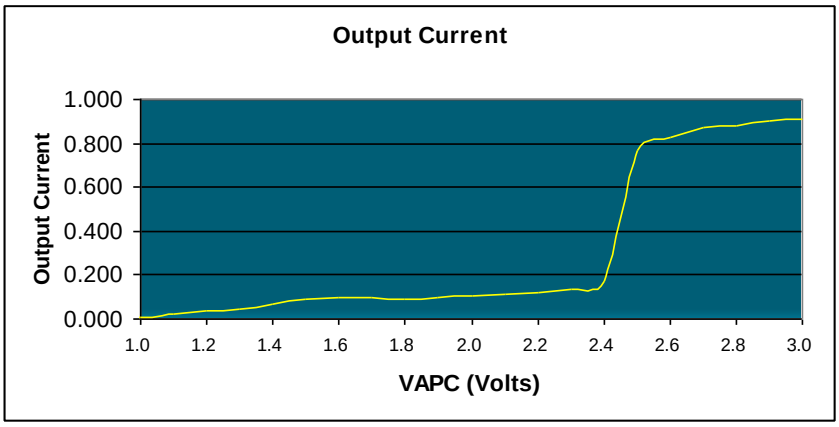


Fig. 24

Then the final results were:

- **Maximal current 0.88Amps instead of 1 Amp, it means less power consumption around 2.9Watts**
- **Maximum output power at 4dBm input power 31dBm, instead of 27dBm planed on the original design**
- **Efficiency of 43% instead of 40.8% planed**

6.2.2 Amplifier

This module was not considered in Phase A, then the implementation was direct from the PCB due to a previous simulation. The gain expected of this circuit was 12dB after the filter, to amplify the FM-Modulator's output planed at -8dBm to have a final input's Power Amplifier at 5dBm, it is mentioned in the last section that it is needed at least 4dBm. **The real result was a gain of 13dB at the output of the filter.** These results are shown in Figure 25.

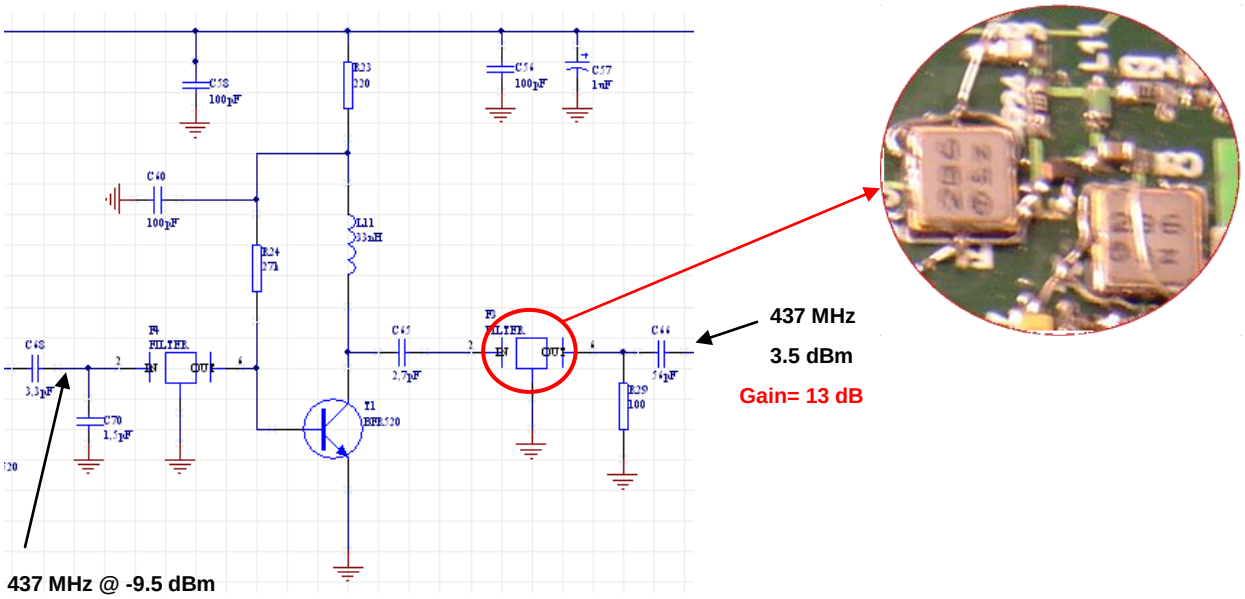


Fig. 25

The test input power was -9.5dBm, but it was grater (Around -8dBm) in the real output of the FM-Modulator that is detailed in the next module. As it is shown in the last figure, there is a picture of **the filters inserted in the PCB; they were as floating ground points and it was necessary to ground them manually, this item has been corrected in the new version of PCB.**

6.2.3 FM-Modulator

This module has the goal to receive the data rate signal in base band and make the up conversion directly to the frequency carrier at 437.5MHz. The target points on this circuit are:

- **Develop a circuit with the correct frequency oscillation at 437.5MHz**
- **Identify the voltage to be applied to the varactor to have from this last, the capacitance that makes the correct frequency**
- **One of the most principal aims of this module is to have a voltage oscillation in the varactor's input less than 3.3Volts, because of the input voltage will be provided directly by the microcontroller**

- **Once the oscillation voltage at the varactor has been designed, it most to design the deviation voltage to be provided by the data rate that corresponds at 1KHz, it means to identify the V peak to peak (Vpp) that the data rate most to have**

The first step was to identify the input voltage at the varactor's input and ensure the oscillation frequency was 437.5MHz, and afterwards, identify the active capacitance acting in the varactor to reach this frequency. In Figure 26 the first results are shown.

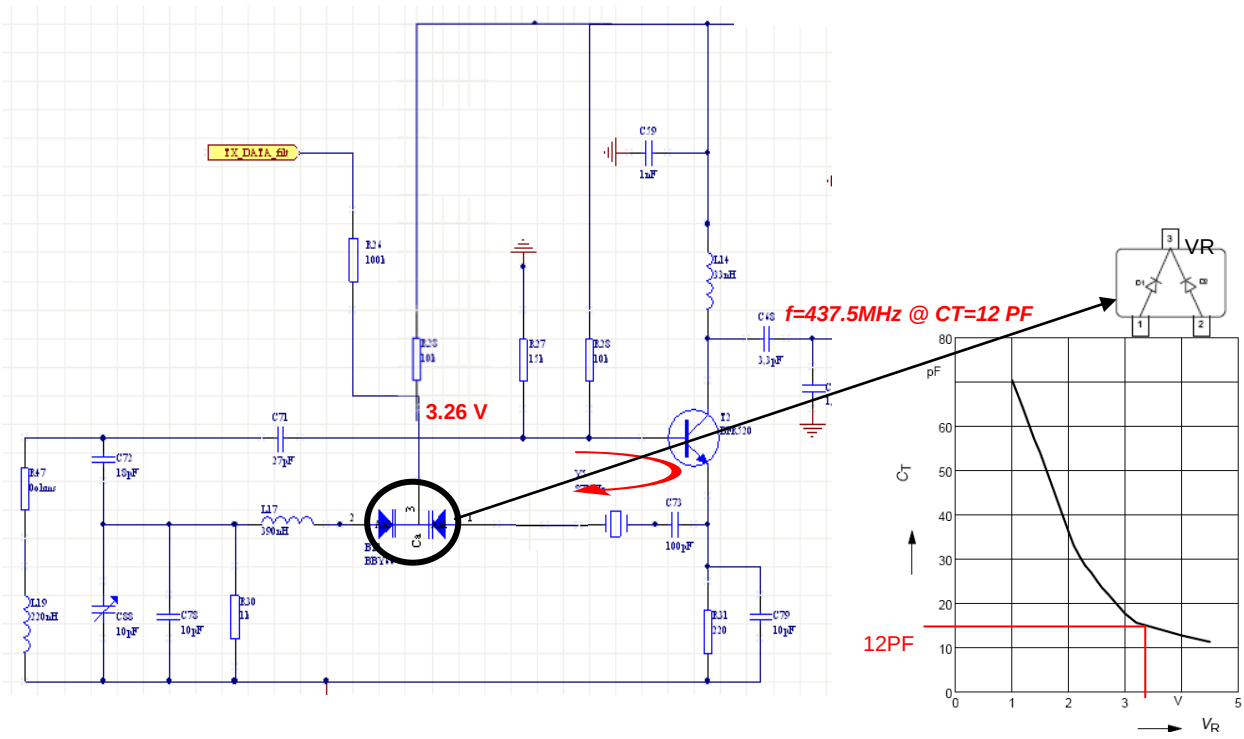


Fig. 26

As this figure shows, the output frequency effectively was 437.5MHz and taking in consideration the data sheet of BBY66 in Appendix A, it shows that the active capacitance was 12pF to produce this frequency and the related voltage at the varactor's input was around 3 Volts, that in fact it was 3.26Volts.

With last results, the first and second goals have been achieved. To reach the third goal it was necessary to decrease the voltage maintaining the stability on the circuit and the main frequency at 437.5MHz. Then a capacitance in series with the varactor has been placed on, to decrease the voltage and to conserve the 12pF of capacitance; the value of this capacitor was calculated in order to have a near voltage of 2.5 Volts and conserve 12pF of total capacitance, the value was fixed at 10pF. The results are shown in Figure 27.

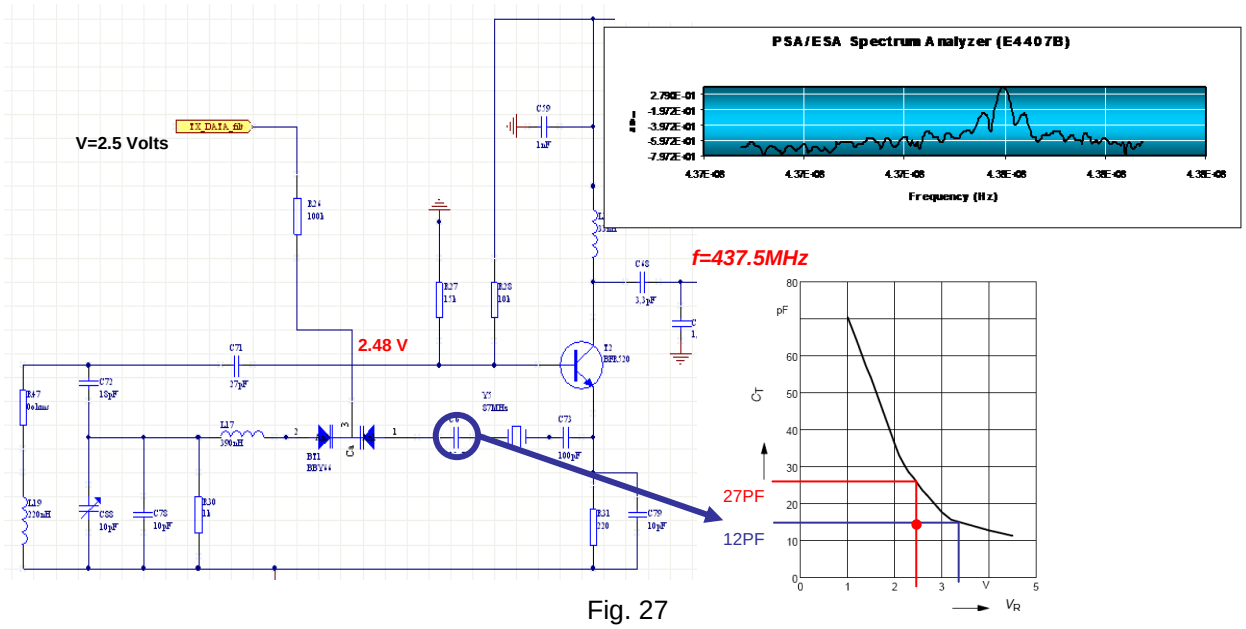


Fig. 27

To achieve the last goal was necessary to identify the Voltage peak to peak of the data rate to generate a deviation frequency of 1 KHz provided by each component, the total deviation is 2 KHz. The procedure was to increment a positive voltage over the 2.5 Volts to know the positive component of Vpp, this value was 0.323 Volts, and the negative component resting the component over 2.5 Volts, this value was -0.361 Volts. It means that the total Vpp was at 0.684 Volts, this is the voltage that the data rate would provide to ensure a deviation frequency at 1 KHz per component. It is important to mention that the filter module after the microcontroller most to provide an offset component to graduate the difference between the valley and peak. The results of this part are illustrated in Figure 28.

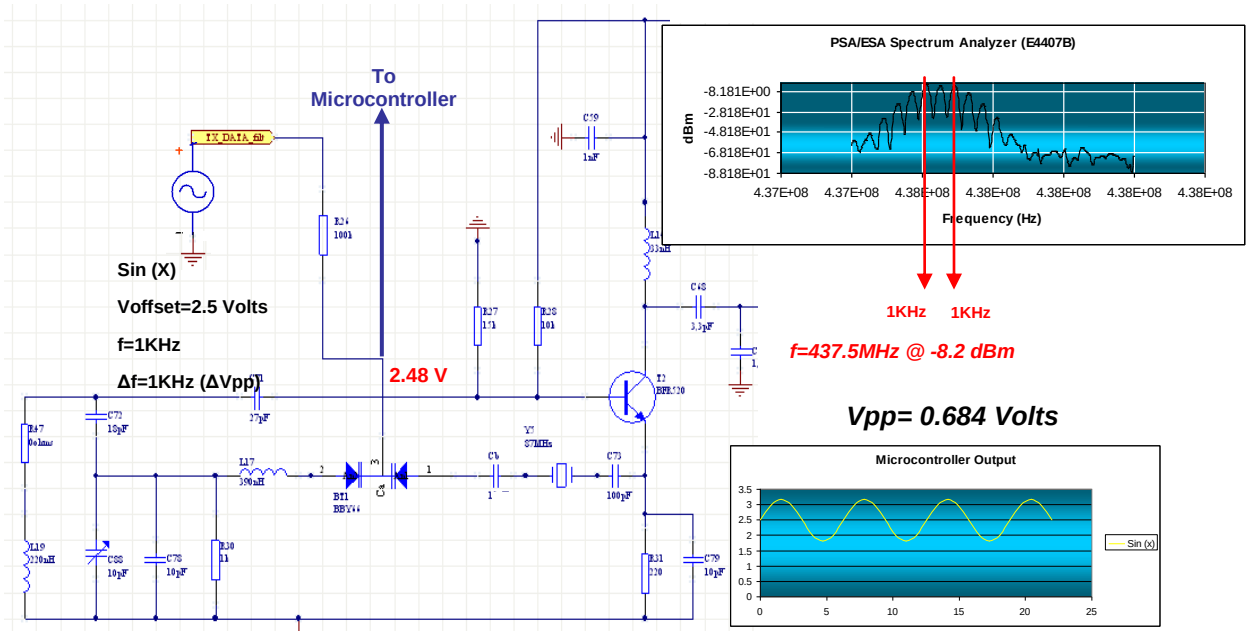
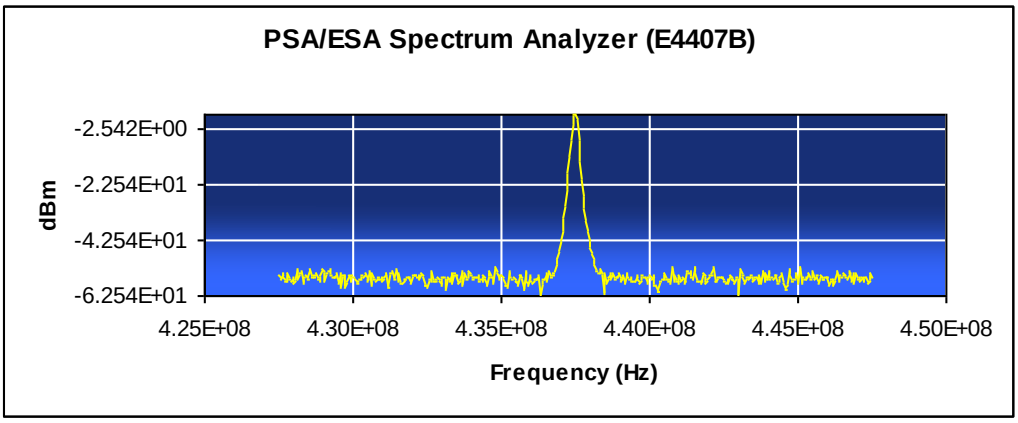


Fig. 28

The data rate signal has been emulated by a sinus signal with rate at 1 KHz and Vpp at 0.684 Volts. **The microcontroller must to give a voltage of 2.48 Volts to the varactor, and the data rate signal must to have a Vpp of 0.687 Volts and provide a small offset voltage to compensate the Vpp components, as it has been mentioned before.** The output signal has a power of -8.2dBm with a total deviation frequency of 2 KHz. This power at -8.2dBm and the gain of 13 dB detailed in the last amplifier point, the input at the power amplifier is in order of 4.8 dBm making the real with the modulation active an

output power from the Power amplifier of 29 dBm, having a difference of +2 dB planed on Phase A. This is shown in Figure 29.



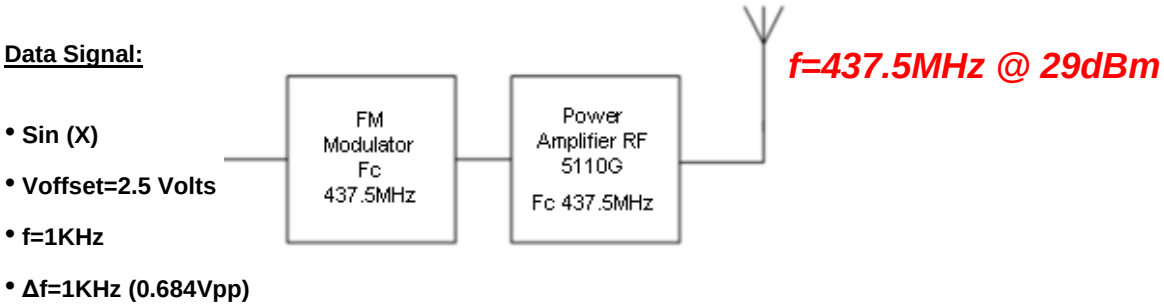


Fig. 29

7 RECOMMENDATIONS

All the recommendations are given in each part or module described above. Nevertheless in the next points are summarized as well as the next steps:

Reception:

- The LNA must be tested with the new frequency at 145.8MHz and tune the best impedance matching to have the maximum gain. The band pass filter must be measured to conserve the lowest loss insertion with a maximum of 1.4 dB
- At the new frequency of 145.8 MHz, within the Mixer circuit is necessary to implement the oscillator at 124.4 MHz and test the output to have 21.4MHz with a minimum power of -40dBm
- All the reception layer must be tested emulating the real environment and the interaction with the modem
- All the changes in the reception layer have been implemented in the PCB file of "Altium Designer" and stored in the new file "PCB_Erivera_December07.prjpcbStructure"

Transmission:

- If it is required to increment the output power of Power Amplifier, it is necessary to increment the gain of the amplifier module before it and work with L13 and L15 of Power Amplifier
- The Microcontroller needs to provide a voltage of 2.48 Volts into the varactor's input and the filter after the data rate must provide a Vpp signal of 0.684 Volts with an Offset voltage to compensate the difference between valley and peak. The filter needs to be precise and flexible to adjust the Vpp to increase or decrease the deviation frequency if it is needed

- If it is required to decrease the input voltage in varactor, it is necessary to analyse in detail the feedback circuit to interact with the capacitance C88 and ensure the frecuency at 437.5MHz
- It is important to consider the heat dissipation on the Transmission layer, specifically in the Power Amplifier circuit. It is necessary to contemplate good dissipation infrastructure between the boards in the Spacecraft
- It is necessary to test the Transmission layer with emulating the real environment and the interaction with the microcontroller and filter
- All the changes in the transmission layer have been implemented in the PCB file of "Altium Designer" and stored in the new file "PCB_Erivera_December07.prjpcbStructure"

As immediate actions it is necessary to test this prototype shown in Figure 30 with the modem in the case of receiver and with the filter after microcontroller in the transmission case and develop the new PCB with new changes.

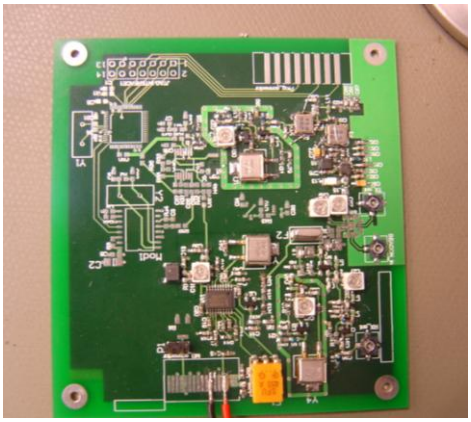


Fig. 30

8 CONCLUSIONS

The original design was finished after the report of Phase A, then some parameters were not included in Phase A report, but they were included in the PCB file, that was helpful to follow the new changes on the design after phase A.

In this project, there were important changes basically in:

- Receiver:
  - LNA
  - Band Pass Filter
  - Demodulator
- Transmitter:
  - Power Amplifier
  - FM Modulator

Very important basic knowledge was developed on each module implemented and improved; this knowledge must be delivered in a clear sense to the future students to reduce the learning curve.

This project has been developed in 11 weeks with 12 hours per week. It is important to mention that to decrease the implementation time, it is necessary to reduce the learning curve of each new student whom will take the project; as a recommendation, it would be helpful to have a meeting to expose the latest work and results in addition to give her/him the latest report.

9 REFERENCES

9.1 Normative references

[N1] http://www.mit.edu/~dluca/publications/daniel_proj_1999_microwave_lna.pdf

[N2] http://www.plextek.co.uk/papers/mixers2.pdf

[N3] http://datasheets.sinus.cz/sosni.php?id=2649

[N4] http://www.rfm.com/corp/appdata/ook.pdf

[N5] http://www.atis.org/tg2k/_quadrature_amplitude_modulation.html

9.2 Informative references

[R1] http://www.orbanmicrowave.com/App_Note_GPS_LNA.pdf

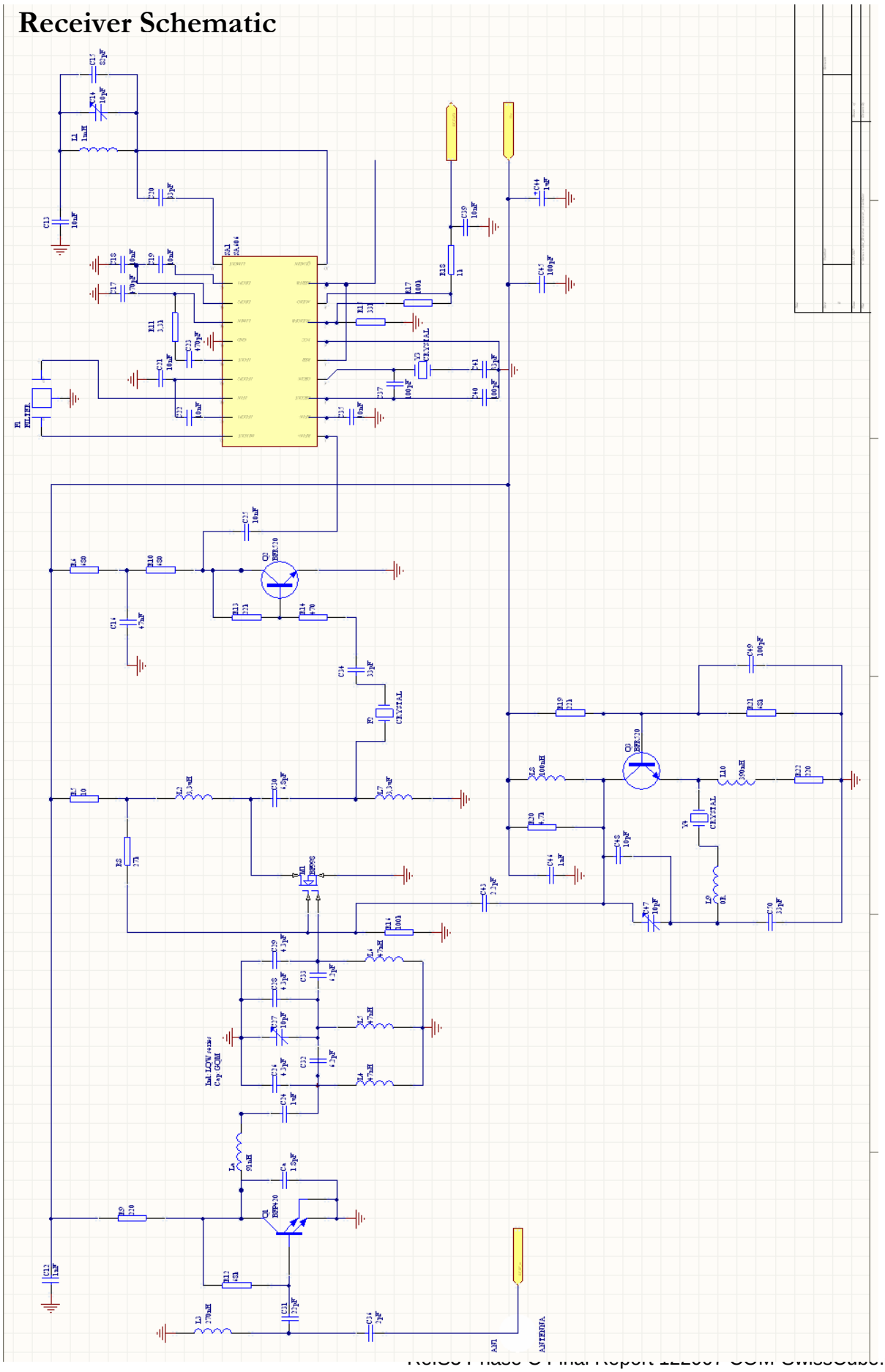
[R2] http://www.nxp.com/acrobat_download/applicationnotes/AN1000.pdf

[R3] http://swisscube.epfl.ch/

Appendix A Data Sheets

Appendix B Schematics

Receiver Schematic



Transmitter Schematic