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Phase A

Design of RF system for CUBESAT

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FOREWORD:

This report is intended to give a description of RF system designed for the spacecraft section of CUBESAT. This report is structured as follows, starting with a basic introduction to CUBESAT and its purpose followed by RF system specifications and finally RF architecture description.

An overview of the communication procedure between CUBESAT and the ground station is described in Chapter 1.

Chapter 2 presents the link budget analysis and the specifications used for this project

Chapter 3 deals in detail on architecture of receiver and transmitter subsections. Functionality of various blocks in the architecture is described. Detailed analysis of each block both from basic principle and circuit realization is given, which is termed as theory section in this project. Once with the adequate theory, practical result is followed.

Appendix A gives a short introduction on crystal oscillators. Appendix B gives circuit schematic for RF transmitter, receiver and PCB layout for transceiver.

ACKNOWLEDGEMENT:

Design of the RF system for CUBESAT is a very interesting project and equally interesting were the days spent at ESPLAB, IMT. I am thankful to Prof. Farine and Dr Cyril Botteron of ESPLAB, IMT for giving me this opportunity to pursue my master thesis at ESPLAB, IMT.

In a nutshell it was a very good learning experience for me, to know about various issues present in designing a RF system. For this I thank Frederic Chastellain, supervisor of this project. During different phases of the project, he guided me by giving me various inputs. I thank him for teaching me various principles in RF system and sharing with me different techniques on soldering minute components on PCB. I sincerely thank his contribution and making this project successful.

I also take this opportunity to express my gratitude to Prof Herbert Shea of Microsystem lab for space applications at EPFL for his initial inputs.

This acknowledgement is incomplete if I ignore Renato Krpoun for his various inputs at different phases of the project. Above all, I owe him more than thanks for introducing this group to Mr.Holger, whose design for time constraints was taken as the base for the design of this system.

I also thank Dr. John Farserotu of CSEM, Neuchatel for his discussions and also everyone who has been involved directly and indirectly in this project.

Prakash Egambaram Thoppay.



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1 INTRODUCTION:

Space equipments are always an interesting area to work on for the amount of challenges it poses; as one has to pay attention to numerous factors during the design. This difficulty makes it the most interesting area at the same time making it a toughest one.

Wide ranges of satellites are there depending on the functionality, Cubesat is one such satellite. A Cubesat is a type of space research picosatellite with dimensions of $10\times10\times10$ cm (i.e., a volume of exactly one liter), weighing no more than one kg, and typically using commercial off the shelf components. Amateur community show a considerable amount of interest in such satellites. There are different sub-systems present in a Cubesat all are fitted in this small cube. Payload refers to the task the Cubesat has to undertake during its mission. The main sub-systems of a CUBESAT are the payload module, power supply module and the module used for communication purpose. Each sub-system is interesting, in its own dimensions. Communication system in a satellite is very important, as the failure of the communication system means the purpose of the mission cannot be achieved. Thus communication sub-system is the vital part of a satellite. The goal of this project is the design of this particular sub-system of a CUBESAT.

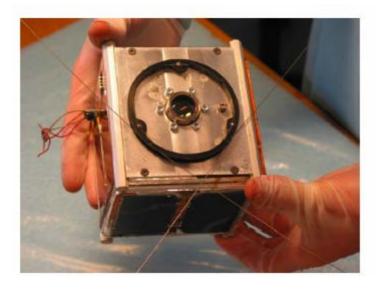


Figure 1-1 CUBESAT

1.1 CUBESAT Program and operation of communication subsystem:

Recently considerable amount of interest has been shown by various universities in designing CUBESAT. The main reason is due to the economics behind realization of Cubesat making it more attractive than the standard satellite. At the same time CUBESAT projects expose students and others involved to gain space design expertise.

Quite a lot of universities have shown considerable amount of interest in designing Cubesat. Rincon cubesat by University of Arizona [1], NCUBE by Norwegian universities [2] and AAUSAT by AALBORG university [3] to name a few. Going through different design documents of these universities gives an idea on different problems that need to be addressed in designing a Cubesat.





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This project involves in the design of the communication sub-system for CUBESAT planned by EPFL. So in further discussions major emphasis is given to the communication sub-system. Communication subsystem has two parts beacon and data transmission. Beacon is used to identify the cubesat; meaning by it emits certain Morse code continuously which acts as a signature for a particular cubesat. By decoding beacon signal one identifies the Cubesat and then starts data communication.

Data communication as the name suggest used to transmit data obtained by payload module to ground station. Also it decodes the command signal from the ground station.

Many universities which carry out such CUBESAT projects buy off the shelf communication equipment for the ground station and design on their own RF system for spacecraft.

As said earlier, ground station equipment is bought as off-shelf radios from manufacturers like Yaesu or ICOM. Ground station equipment has several functionalities. As one knows there is relative speed difference between earth and satellite and due to this, a Doppler shift is present in the received signal. This Doppler shift should be corrected and this correction is done by the ground station receiver. Ground station radio is capable of tolerating the Doppler shift and is able to find out the frequency shift from the received signals, thus the uplink is pre-corrected thereby overcoming Doppler shift problem.

Another important discussion is whether simplex or duplex communication is used. Simplex communication has an advantage in the spacecraft as one doesn't need separate antennas for receiver and transmitter. But as per guidelines Cubesat should be controlled independently by the ground station at any time during the orbit. This is because if the Cubesat is stuck in the data transmit mode then emitting huge power in this band might be potential problem to other users of the same band. Also waiting for the battery to drain out for the cubesat to hopefully start in the receive mode is not acceptable. Thus simplex communication is generally not recommended. Detailed discussion on simplex communication its pros and con can be obtained from reference [4].

The frequencies of Cubesat are in the amateur band for space communications. Hence care should be taken to not to pump more power in this band to avoid distortion of other signals.



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2 CUBESAT COMMUNICATION SYSTEM ANALYSIS:

This section is presents different parameters that are used to calculate link budget and the specifications given for designing the spacecraft's RF transceiver system. Before designing any communication system, link budget analysis is to be calculated. This link budget analysis gives an idea on the different types of losses in the system. A positive link budget means there is a high probability for reliable communication. For computing link budget, the specifications of the system are necessary as link budget margin is dependent on specifications. Thus before introducing link budget analysis, specification of the transceiver system are summarized.

2.1 Specification of CUBESAT transceiver:

For any communication system the important parameters that are to be known before designing are power, data rate and types of modulation.

2.1.1 Power Consumption:

Since there are power constraints in space segment of CUBESAT, power consumed by the transceiver must be minimized. There are two communication system in the space segments, beacon and communication system used for data transmission. The maximum power that can be consumed during data transmission is 2-3W. Since amateur band is used for data communication care has to be taken in amount of power that is transmitted, to prevent distortion of signals in adjacent frequencies.

For uplink, power is not a main criteria but high power might distort signals in adjacent frequencies. Usually allotted power is within 10-20W range.

2.1.2 Data Rate:

Data rate for communication is 2400bps both uplink and downlink. The data rate is decided by modem. The price one has to pay for higher data rate is noise, since higher bandwidth has more noise power, which is explained in detail in link budget section.

2.1.3 Frequency of Operation:

Uplink and downlink communication have different frequencies, uplink frequency is 145MHz and downlink frequency is 437.5MHz. Reason for having downlink frequency higher than uplink is because downlink communication involves transfer of payload and uplink is usually command signals. Since transmitting data over the command signals might need higher data rate in future, 435MHz band is chosen.

2.1.4 Type of Modulation:

Modulation has several important advantages from bandwidth and power point of view. So choice of modulation is important. Two types of modulation were considered for this project Frequency shift keying (FSK) and Phase shift keying (PSK). The choice between two was based on power vs. complexity of implementation.

Figure 2-1 shows probability of error for different modulation schemes. From the figure it is clear that BPSK is superior when compared to BFSK. But from the implementation complexity aspect, BFSK is much simpler and hence used in this design.





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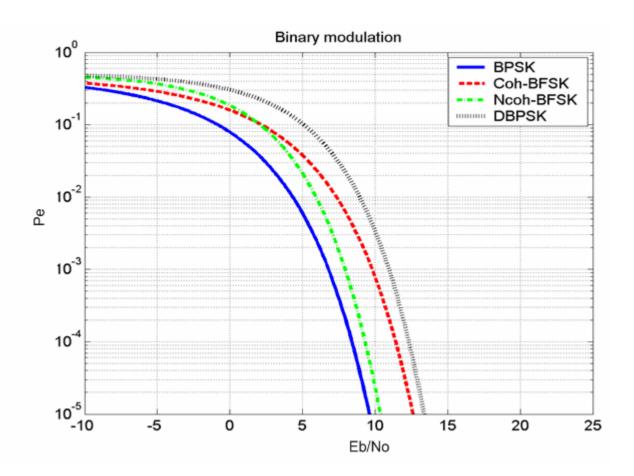


Figure 2-1 Comparison of Pe and Eb/No

2.2 Link Budget Analysis:

Link budget analysis is an important calculation for a communication system. Positive link margin is needed to have reliable communication. This also gives an idea on the different losses that are present in the communication system, hence one is able to concentrate on the dominant loss contributing factor and reduce it, if possible. Downlink and uplink link budget analysis are explained below.

2.2.1 Downlink Budget analysis:

As described in section 2.1.1 due to power constraints, transmitted power is less than 1W leading to stringent margin. Figure 2-2 shows the transmitter system in the space segment of CUBESAT.

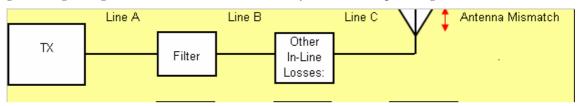


Figure 2-2 Transmitter system representation in space segment

Figure 2-2 also indicates origin of transmission losses during transmission. Lines A, B, C contributes to transmission losses. Also one should note that the space segment antenna is isotropic antenna leading to antenna pointing loss.



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Figure 2-3 Downlink link budget analysis

Figure 2-4 Uplink link budget analysis

Two methods are used to calculate the minimum SNR needed to have reliable communication, they are Eb/No and SNR method. Out of these two methods, SNR method is more stringent when compared to Eb/No. Hence the SNR method is preferred. Margin of 10dB is intended to have reliable communication. In Figure 2-3 SNR calculation method data rate of 1200 bps was assumed. To achieve 10dB margin minimum 0.7 W is to be transmitted as can be seen from the link budget sheet. Another important problem in downlink is the ground station receiver bandwidth calculation. Assuming FSK modulation for transmission, the minimum receiver signal bandwidth is twice the data rate. Thus, if one needs higher data rate, the receiver bandwidth is increased thereby increasing the noise power, reducing the link margin. Therefore, receiver bandwidth is the bottleneck for higher data rate in downlink transmission.



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2.2.2 Uplink budget analysis:

Uplink budget is not as stringent as downlink since there is no restriction on power consumption in the uplink. Figure 2-5 gives an overview of the uplink transmitter; this figure gives an idea of the transmission loss. Unlike the spacecraft transmitter the transmission loss in the ground station is comparatively high due to long wire between antenna and the transmitter block.

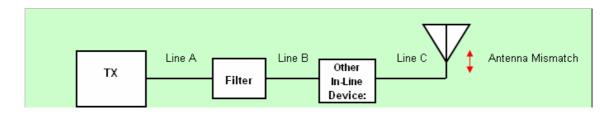


Figure 2-5 Transmitter system at Ground station

Uplink budget sheet is shown in Figure 2-4. The different parameters used to calculate the link budget are similar to downlink as in Figure 2-3 except for the transmission losses are different in uplink as lines A, B, C are longer. Figure 2-3 and Figure 2-4 gives an idea of link budget analysis. In uplink data rate of 9600 bps is assumed because usually the command information is of higher data rates in comparison to downlink data transmission. As one can see from the uplink budget, the power that is transmitted is large and this is possible as there is no power constraint in uplink. Minimum power that is needed to be transmitted can be reduced by reducing the data rate. As data rate increases, the spacecraft receiver noise bandwidth increases.



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3 COMMUNICATION SYSTEM ARCHITECTURE

There are different ways of implementing a particular communication technique; choice of architecture greatly depends on ease of implementation, the cost and more unexpectedly on the availability of components used in the circuit.

In this project as said earlier FSK modulation is used, the architecture used for the receiver is a dual-conversion receiver. In the transmitter the carrier is modulated by the incoming FSK message signals. Before discussing transmitter and receiver architecture, general introduction in block level is given.

3.1 Transmitter Architecture:

The architecture used for transmission is shown in Figure 3-1, the micro-controller sends data to the modem. The modem which can be used is MX614 or CMX469 depending on the data rate. MX614 is a FSK modem capable of transmitting data rate up to 2400 bps. CMX469 is capable of transmitting data rate up to 4800 bps. Modem communicates with the micro-controller and converts the data from digital form to analog form. This can be thought of as an Analog to digital converter but it has extra functionalities like synchronisation with the micro controller etc. This converted FSK signal is then passed through the FM modulator.

The carrier frequency 437.5 MHz; is generated by the local oscillator and it is modulated by the signal received from the modem. The generated FM signal is then passed through a power amplifier. The power amplifier is capable of transmitting 28dBm (>0.5 W). This is required to satisfy the link budget requirements for BER<10⁻⁴. The power amplifier used is RF5110G manufactured by RF micro devices.

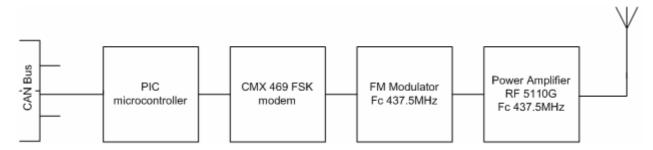


Figure 3-1 Transmitter Block diagram.

This ends a general description of the transmitter architecture used for this project. Detailed description on the implantation of the proposed technique in circuit level is as follows.

3.1.1 Transmitter Architecture realization

Figure 3-1, shows major circuits that are to be designed: the FM modulator and the power amplifier. First, let us see in detail on the working of the FM modulator used to realize this.

3.1.1.1 FM Modulator-Theory:

The FM modulator can be broadly divided into two parts, one generating the carrier frequency and second modulating the carrier with the message signal. The circuit shown in Figure 3-2 is use to generate the FM modulated signal. The oscillator used to generate carrier frequency is of Butler





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configuration. The purpose of different components used in the circuit and principle of operation is explained.

• Principle of operation:

The frequency of oscillation depends on the fundamental frequency of the quartz crystal. Fundamental frequency of the quartz crystal ranges from 20-30 MHz above which the dimensions of crystal become small making it difficult to fabricate. Although, recently innovative ways have come, for fabricating higher frequency quartz crystals but such crystals are very expensive and are very susceptible to vibrations. Therefore they cannot be used for space applications. So, to generate frequencies larger than 30 MHz, overtone property of quartz crystal is used. Every crystal oscillates at fundamental frequency and at every odd harmonic of its fundamental frequency. This overtone property is used to generate higher frequencies.

But in this case, the carrier frequency is at 437.5MHz; at this frequency overtone crystals are not available. So, to generate such high frequencies oscillator configuration is chosen intelligently such that it generates harmonics of crystal fundamental frequency. Common emitter butler configuration is used to generate harmonics because it is stable over wide range of frequencies [5, 6]. The crystal oscillator fundamental frequency is chosen such that 437.5MHz is a harmonic. Frequency spectrum at the output node consists of fundamental frequency and its harmonics. This signal is passed through a SAW filter to filter out 437.5 MHz signal.

Like any oscillator there is an amplifier part and a feedback circuit. The feedback path is from the emitter to the base. The crystal oscillator in the feedback path allows only the fundamental frequency of crystal to pass thorough it, thus acting as a filter at single frequency. The Inductor L22 and capacitor C66 and C67 form a LC tank circuit. This configuration without the varactor and the inductor L22 generates carrier frequency. The carrier frequency is modulated by the LC circuit formed by the inductor L22 and the varactor D2. The varactor diode D2 is a three pin device and biased at a DC voltage, the message signal is applied over the DC bias which changes the capacitance of the LC circuit, thereby modulating the carrier.

• Purpose of different components:

o Capacitors C59 and C56:

These capacitors are used as DC blocking capacitors, hence doesn't change the quiescent point of operation.

o Inductor L20:

If we see the equivalent circuit of the crystal oscillator, there is a shunt capacitance, Cp (Refer Appendix A). The capacitor Cp might influence frequency of oscillation at high frequencies; hence to resonate with this capacitor, a parallel inductor is added.

o Resistor R20 and Capacitor C58:

The resistor R20 is used to fix the bias current for the transistor and having this resistor will dampen the oscillation, hence to suppress influence of resistor at higher frequencies a capacitor is used. The value of capacitor is such that the impedance of the capacitor is very less when compared to the parallel resistor.

The rest of the circuit (Resistive network, Inductor in collector path), are used for biasing and to prevent higher frequencies reaching the DC supply respectively.



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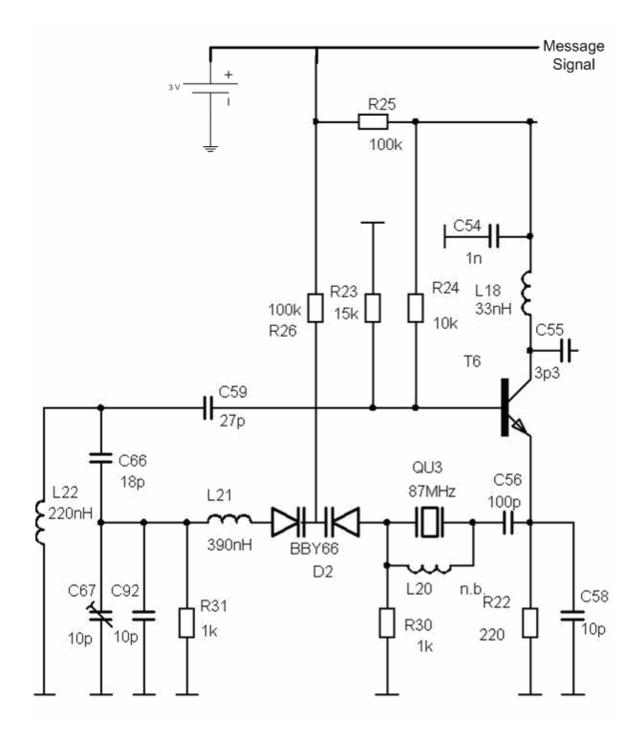


Figure 3-2 FM modulator circuit.

3.1.1.2 FM modulator-Practical results:

To test the functionality separate test board for Figure 3-2 was realized. BBY66 is the varactor diode used to control the capacitance and hence modulate the carrier frequency generated by Butler configuration.

BBY66 component was not available while conducting the test procedure. Hence, modulation of carrier signal was not tested.



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11:42:57 Feb 13, 2006 Mkr1 437.50275 MHz 29.23 mV Ref 141.1 mV Atten 10 dB Peak Log 10 dB/ S2 FC AΑ Center 437.5 MHz Span 100 kHz #Res BW 1 kHz VBW 1 kHz Sweep 128.8 ms (401 pts)

Figure 3-3 437.5 MHz carrier frequency signal.

The output was measured using frequency analyser to confirm the frequency of oscillation. Usually frequency analyser has input impedance of 50 Ω with this input impedance, the oscillator circuit might not start-up. This can be overcome by using probe, since a probe has very high impedance, therefore it won't disturb the circuit.

Figure 3-3 clearly indicates that the frequency of oscillation of the FM modulator circuit is 437.5MHz. Probe used for viewing this is a 10:1 decimator. Hence the amplitude indicated in Figure 3-3 should be multiplied by 10. So the amplitude of oscillating signal is 0.3V. This output signal is passed through an amplifier before sending it to a power amplifier.

3.1.1.3 Power Amplifier-Theory:

Next important part that follows the FM modulator is the power amplifier. Since, the transmitter is designed for the spacecraft, considerable amount of attention should be given to power consumption. Though it might be tempting to send more power to have high margin but it is not possible as the available power is a constraint. So, efficiency of the power amplifier should be good (40-45%). Also in the space, sufficient precautionary measures are to be taken for dissipating the heat generated by power amplifier. Transmitting high power generates more heat making difficult to dissipate (Taking into account the fact that power amplifier have 45% efficiency).

As per the link budget analysis to have 10 dB margin in downlink, the transmitted power should be 27 to 30 dbm. To have power amplifier with such huge output power was a daunting task. Also the number of chip manufacturers designing chips for such specifications were few and to obtain chips in small quantities was not possible. After rigorous search, RF5110G RF micro device power amplifier chip was used for performing this function.

Before going in detail on the circuit used for this design, a general introduction to the power amplifiers is given. Power amplifiers can be divided into several classes mainly depending upon the efficiency of the configuration. Class A, Class B, Class C, Class AB are quite well known



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configurations. Important parameters of a power amplifier are power efficiency, gain and output power.

The RF5110G power amplifier chip is designed for GSM applications but can also be used for 435 MHz frequency band with a degraded efficiency and maximum output power. Figure 3-4 gives the circuit that is used for realizing the power amplifier circuit with RF5110G.

The inductor L4 and capacitor C11 forms the matching network between output of RF5110G and 50 Ω antenna. The output impedance of the power amplifier as seen from the antenna can be obtained from the data sheet.

The use of inductor between the DC power supply and RF signal is to have a high impedance path for the RF signal. Beware as this being power amplifier, RF blocking inductor at the output should be capable of carrying 1A. The output power can be controlled by tuning the voltage on the VAPC pin. One can refer to the datasheet on the dependence of output power on VAPC pin. The input impedance at the input is 50 Ω , making it easy to connect it from earlier stage. A note of caution, since the power amplifier draw considerable amount of current from the power supply; VCC pin should be directly connected to the power supply.

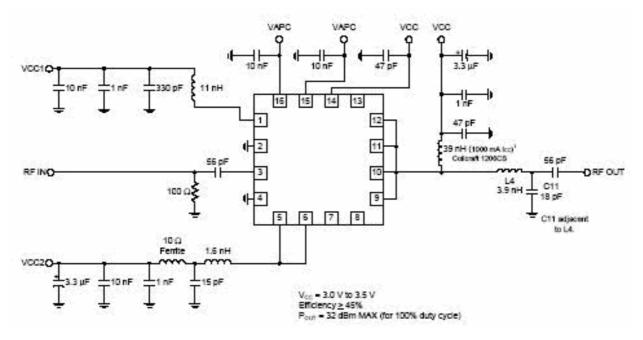


Figure 3-4 RF5110G -Power amplifier circuit

In a power amplifier, maximum output power that can be achieved also depends on the output matching network. Usually the components for the matching network are chosen as per the datasheet to have desired performance. One needs to pay attention on the placement of the matching components as the frequency of operation is high. The components should be placed as near as possible, since the track between the components act as lumped LC circuit and affects the matching thereby degrading the performance. Also power supply track to the power amplifier is to be made wider to carry large currents.

To dissipate the heat generated by the power amplifier, vias are placed at the centre of RF5117G footprint on the PCB layout. These vias are connected to the ground plate. The backside of RF5110G package is soldered to these vias. Thereby the heat generated by the power amplifier is dissipated through these vias to the ground plate.



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3.1.1.4 Power Amplifier-Practical results:

The characteristics which are interesting in a power amplifier are maximum output power, efficiency of the amplifier and gain for various input power. Required output power for a given transceiver system is given by the margin needed for reliable communication. From Figure 2-3 and the specifications one sees that around 0.7 W (i.e. 28dbm) is needed for having 10dB margin.

Power amplifier functionality is tested similar to testing of other blocks; a separate test PCB for power amplifier is designed. The input pin is connected to a signal generator and the frequency is tuned to 437.5 MHz.

Figure 3-5 shows variation of Pout, Gain and efficiency with respect to input power. From the figure it is inferred that for an input power of 1 dbm, output power is around 28.8 dbm, gain of 27.8 and efficiency is 40.8%. These results are satisfactory, as the required output power needed for 10 dB margin is met.

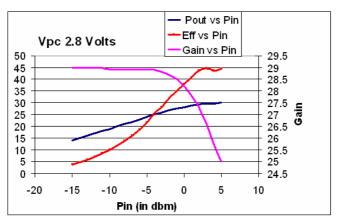


Figure 3-5 Power amplifier characteristics

Figure 3-6 shows the output spectrum of the power amplifier. Since the test measurement is calibrated using a 30dB attenuator at the input of frequency analyser, 30 dB is to be added to the output signal, which results in an output power of 28.8 dbm for Pin 1dbm (taking into account 0.5dB for cable loss).

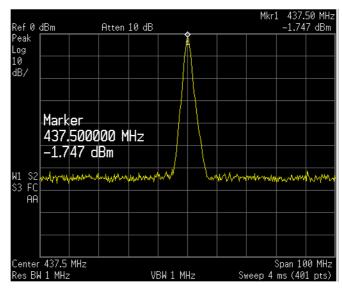


Figure 3-6 Power amplifier output spectrum (with 30db attenuator)



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3.2 Receiver System Architecture:

The receiver design is based on the dual-conversion receiver architecture, which in a nutshell means the received frequency is down converted twice before demodulating the message signal from the carrier.

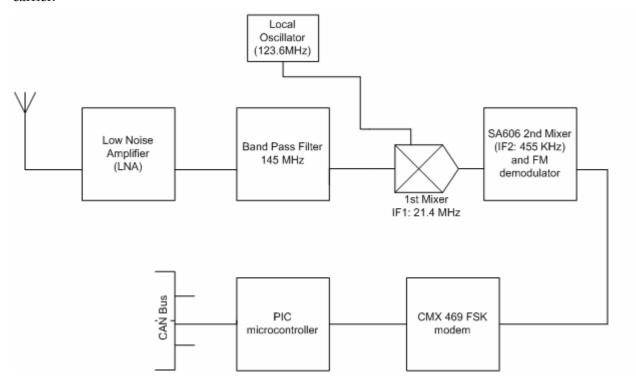


Figure 3-7 Receiver Architecture

Figure 3-7 shows the block diagram representation of the receiver. The major building blocks of receiver are Low noise amplifier, Band pass filter, 1st mixer and final 2nd mixer /demodulator (SA606). The frequency plan of the receiver architecture is, the incoming carrier frequency is at 145 MHz, it is passed through a LNA to boost the signal power while adding less noise to the incoming signal. The amplified signal is passed through a passive band pass filter. After which it is down converted to 1st intermediate frequency (IF1) to 21.4MHz using 1st mixer and local oscillator. Finally, the message is passed through SA606. SA606 is a single IC which includes the 2nd Mixer, IF amplifier and the quadrature FM demodulator. The mixer in SA606 converts the incoming signal to 455 KHz (IF2) before being demodulated by the quadrature detector.

In this project only the RF section is designed. The RF section is followed by baseband section, which consists of CMX469 modem and PIC microcontroller. CMX469 converts message signal into raw bits followed by the PIC microcontroller to understand the bits.

3.2.1 Receiver Architecture Realization:

A detailed overview on the different blocks of the receiver architecture is given. Each section starts with the need for the corresponding block, followed by principle of operation and finally practical results.

3.2.1.1 Low Noise Amplifier-Theory:

LNA as the name suggests is an amplifier which minimizes the noise added during amplification. Figure 3-9 shows noise figure (F_e) calculation for a cascaded system. As can be seen from the



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calculation, the total noise figure is greatly dominated by the noise figure and gain of the initial stage (F1 and G1 respectively). Hence in any receiver architecture the first stage should add as less noise as possible and have very large gain to have better noise figure for the whole system.

So the requirement of a LNA is to add less noise and have large gain. After seeing the need for LNA the basic building block of a LNA are as follows.

The basic components of a LNA are shown in Figure 3-8. A LNA consists of input matching network, amplifier circuit, output matching network and biasing network. Maximum power is transferred from the source to the input of an amplifier; when their impedances have conjugate matching. The matching network between the source and input of an amplifier helps in achieving conjugate matching. The biasing network of the amplifier which fixes its Q-point should be designed in such a way that it doesn't affect the S-parameters during the small signal analysis of the LNA.

The specifications for LNA are given in terms of S-parameters; S21 parameter corresponds to the gain of the amplifier. The S11 (S22) parameter indicates the matching between the amplifier input (output) and source (load).

- S11<-10dB
- S12< -40dB
- S21> as high as possible
- S22<-10dB
- NF=1.5dB

There are practical difficulties in designing a LNA and those that are encountered during this project are summarized below. The S11 and S22 parameters of an amplifier are interdependent due to the influence of amplifier reverse characteristic which is given by S12. So to achieve the specified values of S11 and S22 it is generally recommended to have low Q matching for both S11 and S22, this will reduce the influence of S11 on S22 or vice versa.

The desired values of S-parameters for minimum noise figure and for maximum gain are different. Sopt (optimum S-Parameter) indicates the desired value of S-parameter for minimum noise figure. This value can be obtained by performing a noise analysis using ADS simulator. Generally, to design a LNA having equal S-parameters for maximum gain and low noise figure is very challenging. This can be partially achieved by adding an emitter degeneration inductor.

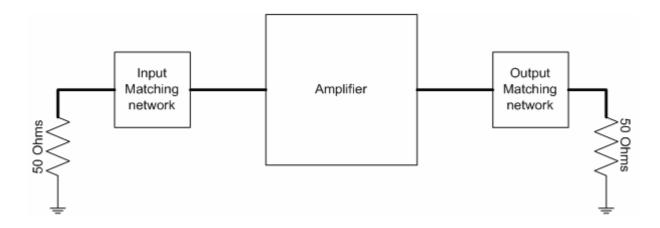
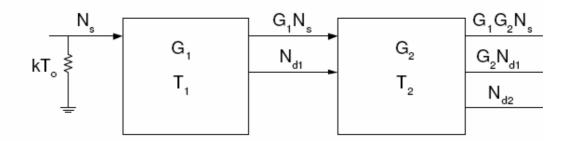


Figure 3-8 Basic Blocks of LNA



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We have at the output of the second device the noise power

$$N_o = G_1 G_2 N_s + G_2 N_{d1} + N_{d2}$$

where

$$G_1G_2N_s = G_1G_2\underbrace{kT\Delta f}_{N_s}$$

$$G_2N_{d1} = G_2\underbrace{G_1(kT_1\Delta f)}_{N_{d1}}$$

$$N_{d2} = G_2kT_2\Delta f$$

Hence,

$$N_o = G_1 G_2 k \left(T + T_1 + \frac{T_2}{G_1} \right) \Delta f$$

Generalization:

$$T_e = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \dots$$

 $F_e = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots$

Figure 3-9 Noise figure calculation



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3.2.1.2 Low Noise Amplifier-Simulation Results:

The results for the LNA shown in this section are calculated using ADS simulator. Figure 3-10 shows the LNA schematic used for simulation. The centre block SP1 is the S-parameter modelling of BFP420. The S-parameters data for BFP420 are obtained by actual measurement using a network analyser. The BFP420 is biased at 1.5V during measurement of S-parameters. The L43, L44, C36 forms the input matching network and C37 and L46 forms the output matching network.

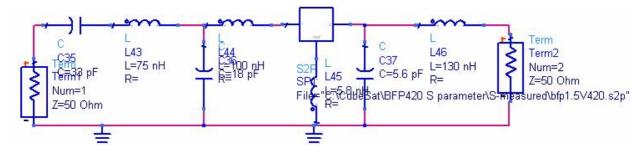


Figure 3-10 LNA Schematic

The S-parameters obtained for the above configuration are shown in Figure 3-11 and Figure 3-12.

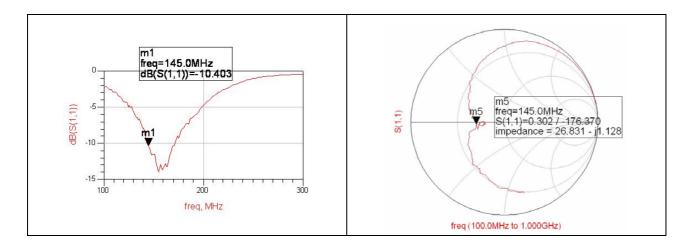


Figure 3-11 S11- Value and Smith chart representation

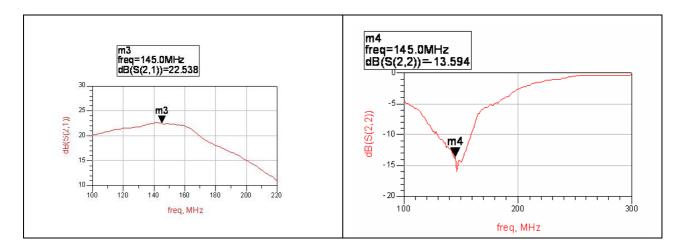


Figure 3-12 S21 and S22 Parameter for LNA



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Smith chart representation of S11 in Figure 3-11 gives the input impedance seen by the 50Ω source. The corresponding value of S11, S21, and S22 at 145MHz are -10dB, 22dB and S22 -13dB respectively. These values meet the specification given in section 3.2.1.1; further to this simulation in ADS, actual analysis of the LNA on a PCB is to be performed to cross check the values obtained. Noise analysis of the above configuration is also to be carried out to find out the noise figure of the LNA.

3.2.1.3 Bandpass Filter-Theory:

The signal received after amplification through a LNA is passed through a Band pass filter. Band pass filter helps in reducing the total noise power in the signal bandwidth. Also, as seen in the receiver architecture Figure 3-7, the signal is passed through a mixer. Mixer design is plagued by the problem of image frequency. This image frequency problem can be overcome by passing the signal through a band pass filter before passing through a mixer. Thus band pass filter can be efficiently used to remove many design issues.

Filters are classified based upon the attenuation characteristics; Butterworth, Chebyshev and Bessel filter. Butterworth filter is a medium-Q filter that is used in designs which require the amplitude response of the filter to be as flat as possible. Chebyshev filter is a high Q filter that is used when steeper descent to stopband is require and passband response need not be flat. In this filter ripples are allowed in passband.

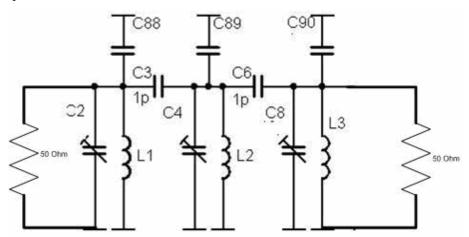


Figure 3-13 Bandpass filter

The bandpass filter designed in this project is of Butterworth type. Figure 3-13 shows the Bandpass filter. In this short description on bandpass filter emphasis is given on following design issues.

- One has to choose between different filter responses characteristics that are available based on the given specifications.
- Load and source resistance is very important as filter response changes depending on these values.
- Generally, for any lumped element bandpass filter, insertion loss and Q is to be specified, these losses are due to parasitic resistances present in capacitor and inductors.
- From S21 parameter, the filter response and insertion loss of the filter can be obtained.
- Bandpass filter attenuates the image frequency.



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3.2.1.4 Bandpass filter -Practical Results:

For characterizing bandpass filter, S-parameter analysis is carried out. The response of a filter can be obtained from S21 parameter. S21 parameter that is obtained for the above configuration is for 50 Ω load and source resistance. The measured S21 parameter for the filter is shown in Figure 3-14.

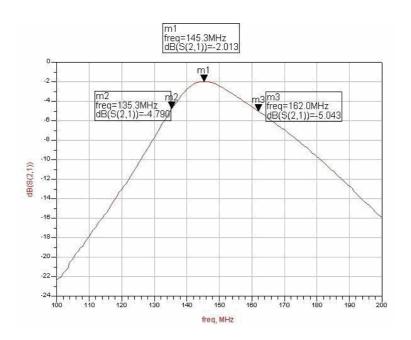


Figure 3-14 Measured S21 Parameter for Bandpass filter.

The results that are obtained from the S21 parameter of Bandpass filter are as follows, 1) The centre frequency of the filter is 145 MHz 2) The 3db bandwidth of the bandpass filter is 27 MHz 3) The Insertion loss of the filter is around 2db 4) The 1st intermediate frequency of the receiver design is 21.4 MHz, hence the image frequency is at 187.8 MHz (F_c+2*IF). The measured value of S21 parameter (Figure 3-14.) indicates that the image frequency is attenuated by -10dB.

3.2.1.5 Mixer and Local Oscillator-Theory:

This section gives an idea about the design of mixer and generation of local oscillator frequency. Before going into the technical details on operation of these modules, mixer details is explained. The input to the mixer is the carrier frequency from the bandpass filter and from the local oscillator. The mixer is designed using BF998 dual gate MOSFET. On the oscillator front, Colpitt configuration is used to achieve desired frequency. Colpitt is particularly interesting because of low phase noise when compared to other configurations.

3.2.1.5.1 Local Oscillator-theory:

Figure 3-15 gives the oscillator configuration used in the generation of local frequency. This module is intended to give information on the practical difficulties that were encountered during the design of oscillator, rather than how to design a oscillator. More on oscillator design can be obtained from other resources [7]. Oscillator design is simple in one sense, satisfy the Barkhausen criteria then you will see your circuit oscillating. But how stable is your oscillating frequency depends on the configuration you use, as phase noise is different for different configurations. Colpitt oscillator configuration is particularly interesting as it adds less phase noise.



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Brief explanations on different components present in the Local oscillator configuration are explained as follows.

• Crystal Oscillator QU2:

The crystal oscillator is used to have high Q response. The crystal used here is in series mode and it is in fifth overtone regime. The crystal frequency is at 123.6 MHz which is the frequency needed for local oscillator. The function of crystal is also explained in Section 3.1.1.1. This crystal acts as a filter and prevents from oscillating in other frequencies. One can refer Appendix A to know more on Crystals.

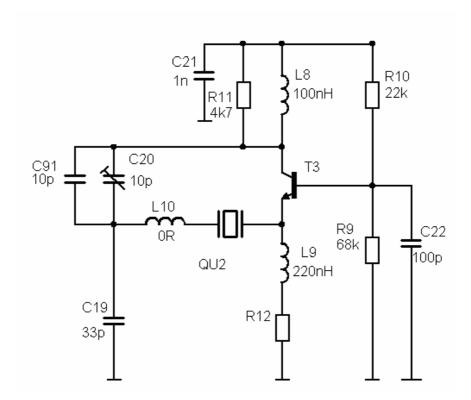


Figure 3-15 Local Oscillator Configuration.

• Inductor L10:

The inductor L10 can be used to pull down the resonant frequency of crystal, but generally it is not advised to have such inductors. The pulling range is also not large, it is typically few KHz.

• C19&C20 and L8:

These components form the tank circuit and hence determine the fundamental frequency of oscillation of the circuit. The value of these components should be chosen such that it satisfies the Barkhausen criteria.

To check whether the circuit is working as expected, frequency analyser is used. There can be several occasions where your circuit will be working properly but wrong settings in the analyser might not show expected results. Hence, it is recommended to know about frequency analyser before testing the oscillator circuit. This point is highlighted because circuit oscillation highly depends on the load resistor. Usually the input impedance of frequency analyser is 50 Ω . Hence with such low input impedance the circuit might not start up, hence one might not see the output, though the circuit



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might work properly. So, it is better to use probe to see the oscillation, as probe has high impedance and doesn't affect the oscillation circuit.

3.2.1.5.2 Mixer Theory:

Mixer is very important in any transceiver architecture, as it helps in up-converting or down-converting the carrier frequency. The principle of mixer is simple, multiplication of two sine waves results in sum and difference components. We are very much interested in difference between the two frequencies, as we are using it as down converter. Usually in a output of mixer, there are other frequency components and hence a filter is usually followed by a mixer which allows only the frequencies that is of interest.

There are several ways to design a mixer, in this project BF998 dual gate MOSFET is used to achieve this functionality. BF998 is a dual gate MOSFET, where control input is given at gate 1 and input signal is given at gate 2. The gate-1 of BF998 should be properly biased to achieve a given trans-conductance. Figure 3-16 shows principle of mixer using BF998 transistor.

The gate 1 is used to control the gain also; hence proper biasing of this gate is necessary to achieve a given performance. As shown in Figure 3-16 resistor R3 and R4 form the biasing network for BF998.Output of a mixer has several frequency components. Hence QU1 filter is necessary to separate the signal component from other frequency components.

The input signal frequency to the mixer is 145 MHz and local oscillator frequency is 123.6 MHz. Given this as inputs to the mixer, expected output is 21.4 MHz signal. This component is filtered out using QU1 crystal filter. The QU1 crystal filter is 21M15A, 2 pole 21.4 MHz crystal filter. Detailed specification can be obtained from www.klove.nl.

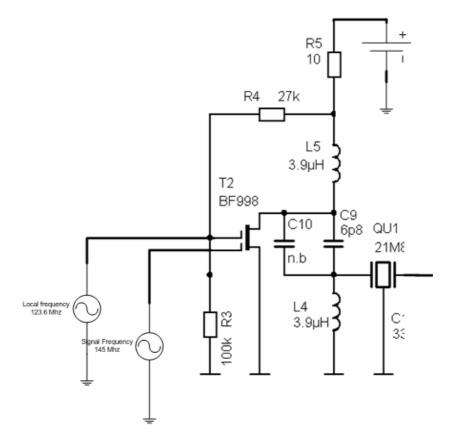


Figure 3-16 BF998-Mixer configuration.



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3.2.1.6 Mixer and Local Oscillator-Practical Results:

The mixer and local oscillator are tested together for their functionality. Figure 3-16 shows mixer along with local oscillator. A separate PCB for mixer and local oscillator circuit is designed for testing the functionality. Input signal frequency of 145 MHz is given from external source to one input of BF998 MOSFET. The other input frequency to BF998 is generated using local oscillator.

Figure 3-17 shows the output of the mixer and local oscillator configuration.

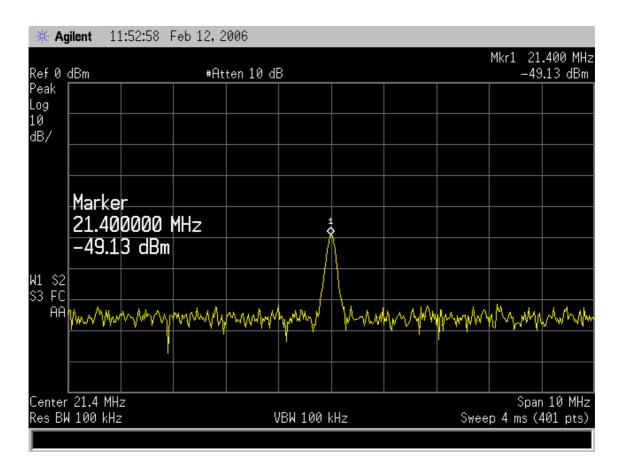


Figure 3-17 Spectrum of Mixer output

The spectrum of mixer output was measured and shown in Figure 3-17. The figure clearly indicates the output at 21.4 MHz which was as expected.

3.2.1.7 SA606 and FM demodulator operation-Theory:

Final and concluding part of the receiver architecture is operation of SA606 chip and FM demodulator. The SA606 chip consists of mixer, limiter and FM demodulator. As said earlier being a dual-conversion receiver architecture, two mixers are needed, 2nd mixer is present within the SA606 chip. The various parts of the chip and its functionalities are explained further.

3.2.1.7.1 2nd Mixer:

Figure 3-18 indicates block diagram of the SA606 chip. This figure includes only the components necessary for the mixer part.

The 2nd intermediate frequency in this case is 455 KHz. One of the input signals is 21.4 MHz from the previous mixer. The other input signal to the mixer is the local oscillator frequency which is



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generated using the oscillator within the chip. External crystal will determine the local oscillator frequency. To have 455 KHz intermediate frequency, the local oscillator frequency should be at 20.95 MHz, the fundamental frequency of the crystal used in this circuit is at 20.95 MHz as required. Capacitor C37; C38 etc are to be chosen correctly so that the oscillator can start up. The detailed procedure of choosing the value of these capacitors can be obtained from Reference [8].

CFWS455E is a 455 KHz centre frequency crystal filter whose 6dB bandwidth is 7.5 KHz. The filter suppresses other frequency components generated by the mixer and allows only the desired signal. The value of the components to be connected at various other pins can be obtained from the complete Receiver architecture in Appendix B.

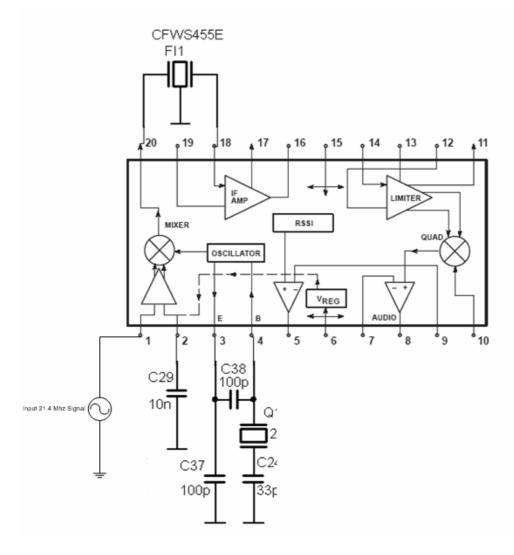


Figure 3-18 SA606 2nd Mixer

3.2.1.7.2 FM demodulator:

There are different ways to demodulate a FM signal. In this project, Quadrature demodulator is used to obtain message signal from the carrier signal. A brief description on the principle of quadrature demodulator is given below.

Figure 3-19 helps in understanding the principle of quadrature demodulator. The aim is to demodulate the message signal from the carrier frequency. Figure 3-19 consists of phase shift network and a phase detector. The phase detector compares the phase of the IF signal (v1) to v2,



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the signal generated by passing v1 through a phase shift network. This phase shift network includes an LC tank (L, Rp, and Cp) and a series reactance (Cs). The network gives a frequency-sensitive 90° phase shift at the centre frequency. Detailed mathematical analysis of quadrature demodulator can be consulted from reference [9].

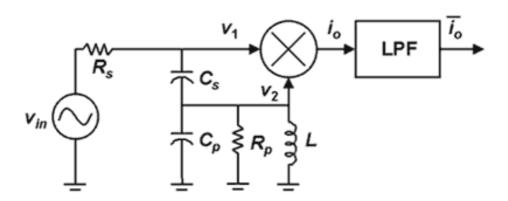


Figure 3-19 Quadrature Modulator Circuit

SA606 uses quadrature demodulator to obtain message signal from the carrier frequency. Input to the quadrature demodulator is square wave. The square wave is obtained by passing the amplified 2^{nd} intermediate signal through a limiter. This limiter converts the intermediate signal into square wave, facilitating quadrature demodulation.

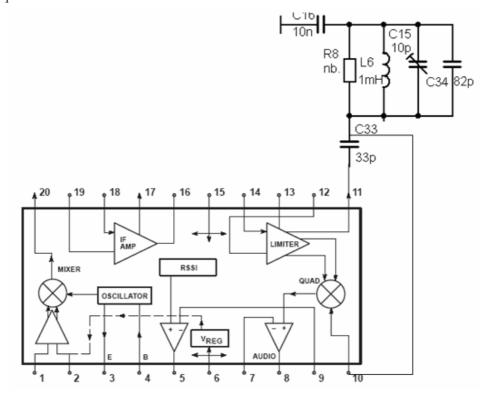


Figure 3-20 FM demodulator

Figure 3-20 shows SA606 circuit along with the FM demodulator circuit. In comparison with Figure 3-19, the phase shift network is formed by L6, C33, C6 and R8. The phase detector is within SA606 IC, which is clearly shown as quad detector.



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The output of demodulated signal is obtained at Pin 8. The resonant frequency of the RLC circuit is tuned for 455 KHz, to have maximum phase shift. The value of various components can be determined from the formula given in Reference [9].

3.2.1.8 SA606 and FM demodulator- Practical Results:

A separate test PCB board for testing the functionality of SA606 is designed. The aim is to test the working of 2nd mixer and FM demodulator. To verify the working of SA606, a FM modulated 21.4 MHz carrier signal is given to input pin of SA606. At Pin 18 of SA606 chip, 2nd intermediate frequency 455 KHz is noticed. Thus, confirming the working of mixer in SA606.

To check the working of FM demodulator, a FM carrier, modulated by swept sine is given as input to SA606. Thus, if the FM demodulator is working properly then we will see sine waves of different frequencies at different instances at the output, confirming the working of FM demodulator. The parameters of the FM carrier signal are: frequency deviation is 4 KHz and the frequency of the input message signal is variable as it is a swept sine.

Figure 3-21 shows the output of the FM demodulator as seen in the oscilloscope. Figure 3-21 shows that there are different frequencies at different time intervals validating the operation of FM demodulator. In practice, the capacitor C34 in Figure 3-20 should be varied to have a centre frequency of 455 KHz.

To get an idea on the sensitivity of the SA606 chip, the input power of the carrier signal is varied. It was found out that for an input power up to -77dbm the output signal was clearly seen, below which the output signal was noisier. But to have a conclusion on the minimum input signal power needed for acceptable BER, can be obtained only along with the baseband section. This is because the modem is capable of detecting the signal even when the input carrier is noisier.

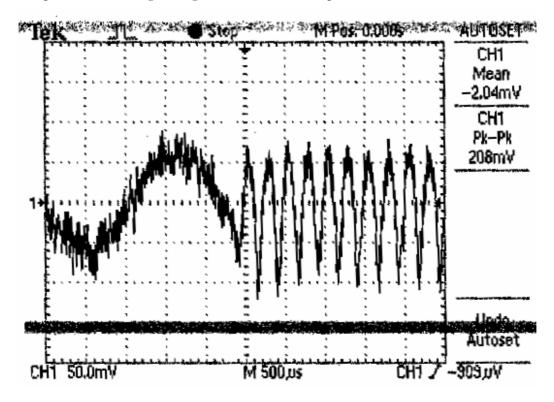


Figure 3-21 FM demodulator output



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4 CONCLUSION AND FUTURE WORK:

In this work a detailed study and experimental verification of the different blocks of transmitter and receiver was carried out. Separate test PCBs were designed for the critical blocks of the transceiver, with these PCBs functionality of each individual block was tested. The results given in the previous section testify that the blocks that were tested are working as expected.

After having reached a satisfactory stage in this project till now, it is quite sure there are still interesting paths ahead. Master board containing the complete transmitter and receiver circuit was designed but the implementation of individual blocks on to the master board needs to be carried out. Further more, complete system performance is to be analysed. Below are some suggestions indicating various tasks that are to be performed for the communication transceiver system of CUBESAT.

- In the spacecraft transceiver, the minimum signal power that can be detected by the receiver has to be determined. This can be obtained by connecting the input of receiver to a signal generator and varying the input power. BER for various input power can also be calculated, this calculation will give an idea on the minimum input signal power needed for decoding with an acceptable BER. At the transmitter end, output power of the amplifier with the FM modulating circuit is to be determined.
- Complete testing of transceiver system involves communicating between ground station and RF spacecraft part. Ground station transceiver can be either ICOM 910H or Yaesu FT817. Both the radios (that is how it is termed in amateur community) provide similar functionality, it would be better to get a view from what other CUBESAT programs have used before finalizing between these two radios. Also, one has to know thoroughly the different functionality these radio stations can provide for space communication. (Supposedly these are bit advanced in comparison to other products). This can help in coming out with new solutions and efficient communication.
- Once ground station and space craft transceiver system are ready, one can start with voice communication to check the performance. Once voice communication is satisfactory, one has to check for data communication with the modem.
- After successful completion of data communication and getting an idea on the BER achieved, emphasis can be given on improving the performance of the system, if needed. This can be achieved by using various error correcting codes prior to data modulation. Comparison on the performance of various error correcting codes can also be carried out to come to a conclusion on the possible error correcting codes that can be used.

These are some of the factors that need to be checked and which are foreseen in this project.





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5 REFERENCES

- 1. Available from: http://cubesat.arizona.edu/rincon_1_sat/.
- 2. Available from: http://www.ncube.no/project_documents.
- 3. Available from: http://www.aausatii.auc.dk/.
- 4. Available from:

http://www.stec2005.space.aau.dk/files/Simplex_Utilization_Small_Sats_RELEASE1.pdf.

- 5. Available from:
 - http://www.semiconductors.philips.com/acrobat_download/applicationnotes/AN1983.pdf
- 6. Available from: http://www.sss-mag.com/pdf/saosc.pdf.
- 7. Available from: http://xanadu.ece.ucsb.edu/~long/ece145b/Oscillators1_w03.pdf.
- 8. Available from: http://www.maxim-ic.com/appnotes.cfm/appnote_number/1210.
- 9. Available from: http://www.techonline.com/community/ed-resource/feature-article/14378.
- 10. Available from: http://www.maxim-ic.com/appnotes.cfm/appnote number/726.







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Appendix A

A.1 Crystal Oscillator basics:

Crystal Oscillator is used in transmitter and receiver to generate carrier frequency and local frequency. This module is intended to give an introductory knowledge on quartz crystals, which will help in debugging the oscillator circuits and also the parameters one has to pay attention during crystal ordering [10].

A.1.1 Crystal Oscillator- Model:

Quartz crystal is modelled as shown in Figure-A.1. It is modelled as a series RLC circuit which determines the resonant frequency and a parallel holder (shunt) capacitance. Parallel capacitance models the parasitic capacitance and plays an important role at higher frequencies. To eliminate the effect of holder capacitance a parallel inductor is connected externally. The inductor value is chosen such that it resonates with the shunt capacitance.

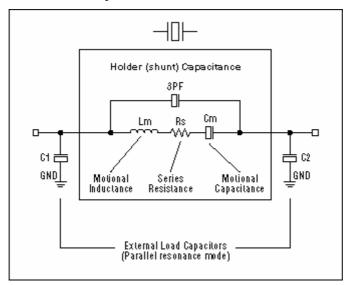


Figure A-1: Crystal oscillator model

A.1.2 Specifying Quartz Crystal:

Specifying quartz crystal is very important, there are many parameters one has to note down before ordering a quartz crystal. The parameters are as follows.

- Resonance frequency.
- Resonance mode.
- Load capacitance.
- Series resistance.





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Any quartz crystal has two different types of mode: series resonance and parallel resonance. Parallel resonance is of slightly higher frequency than series frequency. Series resonance or parallel resonance depends on the oscillator circuit configuration.

The crystal is said to be in parallel resonance when a low capacitance load is used on the crystal. Hence, load capacitance is to be specified while ordering when the crystal is used in parallel resonance mode. Similarly, series resistance is to be specified in series resonant mode. Series resistance is the effective resistive component in series with the RLC model of the crystal (see Figure A-1). Oscillator circuits can tolerate to a certain value of series resistance in the feedback path. A typical range is 25 Ω to 100 Ω for most crystals. The crystal vendor usually characterizes this resistance and specifies typical or maximum values for series resistance. Excessive series resistance can lead to oscillator start-up failure, so sufficient margin must be built in the oscillator design.



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Appendix B

B.1 Schematic and PCB CAD drawings:

B.1.1 Transmitter:

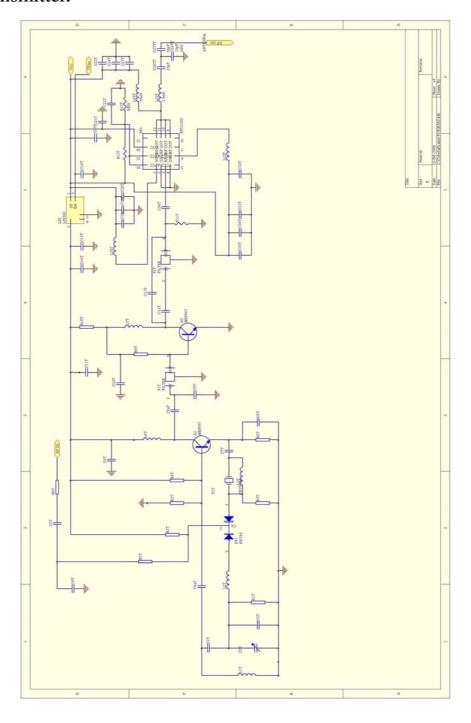


Figure B-1: Transmitter Schematic





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B.1.2 Receiver Schematic:

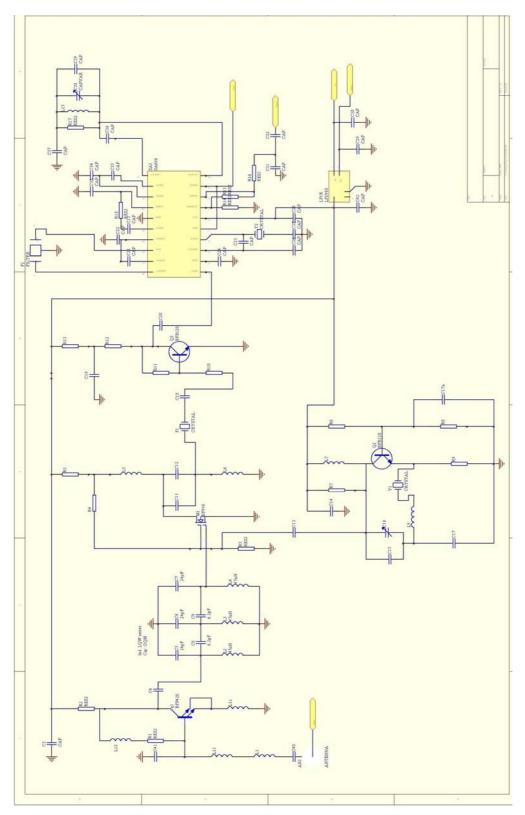


Figure B-2: Receiver Schematic



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B.1.3 PCB Schematic:

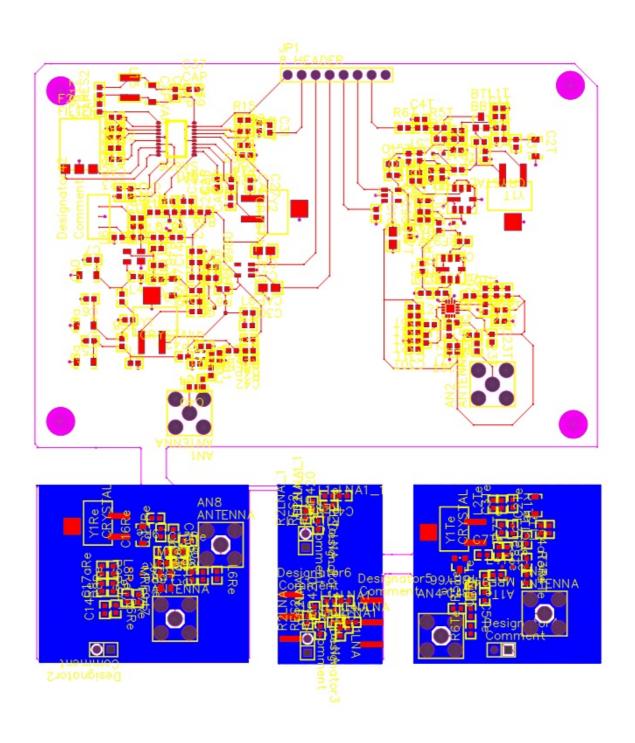


Figure B-3: PCB layout of Transceiver